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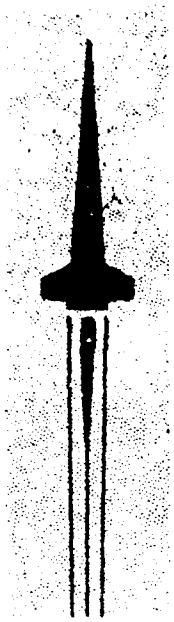

U.S. ARMY MISSILE RESEARCH AND DEVELOPMENT COMMAND

Redstone Arsenal, Alabama 35809

STORAGE RELIABILITY

OF

MISSILE MATERIEL PROGRAM

MONOLITHIC BIPOLAR SSI/MSI DIGITAL

& LINEAR INTEGRATED CIRCUIT ANALYSIS

LC-78-IC1

JANUARY 1978

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HEADQUARTERS

U. S. ARMY MISSILE RESEARCH & DEVELOPMENT COMMAND

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ABSTRACT

This report documents findings on the non-operating reliability of Small Scale Integration (SSI) and Medium Scale Integration (MSI) Monolithic Bipolar Digital and Linear Devices. Long term non-operating data has been analyzed together with accelerated storage life test data and integrated with surveys of device users. A non-operating prediction model has been developed which measures the effect of storage temperature and environmental stress on the devices.

In the comparison of non-operating to operating device characteristics, several data banks and operational prediction models have been analyzed and are also summarized herein.

This report is part of a program whose objective is the development of non-operating (storage) reliability prediction and assurance techniques for missile materiel. The analysis results will be used by U. S. Army personnel and contractors in evaluating current missile programs and in the design of future missile systems.

The storage reliability research program consists of a country wide data survey and collection effort, accelerated testing, special test programs and development of a non-operating reliability data bank at the U. S. Army Missile R&D Command, Redstone Arsenal, Alabama. The Army plans a continuing effort to maintain the data bank and analysis reports.

This report is one of several issued on missile materiel. For more information, contact:

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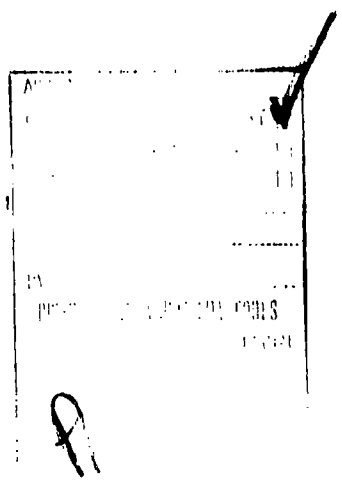

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SECTION 2

SUMMARY

Approximately twenty billion hours of storage or non-operating data has been gathered together with an additional 247 million hours of high temperature storage test data for monolithic bipolar small scale integration (SSI) and medium scale integration (MSI) digital and linear integrated circuits.

A failure rate prediction model has been developed similar to the MIL-HDBK-217B model:

$$\lambda_S = \Pi_L \Pi_Q [\Pi_T C_1 + \Pi_E C_2]$$

where λ_S is the device storage reliability

Π_L is the learning factor

Π_Q is the quality factor

Π_T is the temperature factor

Π_E is the application environment factor

C_1 and C_2 are the base failure rates for time/temperature effects and mechanical stress effects respectively.

Failure rates at 25°C ambient temperature in a ground fixed environment range from a low of 0.875 fits (failures per billion hours) for MIL-STD-883 Class A devices with aluminum metallization/aluminum wire systems to a high of 1178 fits for commercial quality devices with aluminum metallization/gold wire systems.

The development of the models is described in Section 4 and the factors are given in Section 5. Figure 2-1 presents a summary of the models.

The analysis identified a distinct difference in the device storage reliability depending on the metals used in the metallization/interconnection system. Mono-metal systems at the wire bond interface are recommended for high storage reliability.

Figure 2-1.

PREDICTION MODEL FOR SSI/MSI
MONOLITHIC BIPOLAR DIGITAL AND LINEAR IC's
NON-OPERATING RELIABILITY

ALUMINUM METALLIZATION, ALUMINUM WIRE, GOLD POST:

$$\lambda_S = \pi_L \pi_Q [C_1 \pi_T + C_2 \pi_E]$$

π_L = Data Inconclusive (Use MIL-HDBK-217B Factors)

π_E = Data Inconclusive (Use MIL-HDBK-217B Factors)

π_Q vs MIL-STD-883 QUALITY CLASSES	
Class	π_Q
A	1
B	3.5
C	4.5
D	11.25

$C_1 = 0.00135$
$C_2 = 0.00074$

π_T vs Ambient Temperature	
°C	π_T
25°	0.1
30°	0.14
40°	0.29
50°	0.56
100°	8.64
120°	26.28
150°	70.12
170°	141.94

ALUMINUM METALLIZATION, GOLD WIRE, GOLD POST:

$$\lambda_S = \pi_L \pi_Q [C_1 \pi_T + C_2 \pi_E]$$

π_L = Data Inconclusive (Use MIL-HDBK-217B Factors)

π_E = Data Inconclusive (Use MIL-HDBK-217B Factors)

π_Q vs MIL-STD-883 QUALITY CLASSES	
Class	π_Q
A	1
B	3.5
C	4.5
D	135

$C_1 = 0.000034$
$C_2 = 0.00872$

π_T vs Ambient Temperature	
°C	π_T
25°	0.1
30°	0.18
40°	0.54
50°	1.53
100°	119.53
120°	700.71
150°	3332.91
170°	10223.86

GOLD SYSTEMS AND BEAM LEAD SYSTEMS
(To Be Added in Future)

Analyses of device complexity, packaging, aging, quality level, logic type, use temperature, die attach method and glassivation have been performed. Primary reliability characteristics identified from these analyses are storage temperature and the device quality level.

Device construction, failure mechanisms, procurement and use characteristics are identified and are used to classify devices in Section 3.

Principle storage mechanisms are identified and screen and/or quality conformance testing to minimize these defects are listed.

Existing operational failure rate data sources have been reviewed and are described in Section 6. Average operating to non-operating ratios were calculated and range from approximately 5 to 71 for SSI and MSI digital devices and 14 to 71 for linear devices with aluminum metallization and aluminum wire systems. Average operating to non-operating ratios for devices with aluminum metallization/gold wire systems range from approximately 0.5 to 7.1 for SSI and MSI digital devices and 1.4 to 7.1 for linear devices. These ratios are based on the MIL-HDBK-217B prediction model and the non-operating models developed in this report.

SECTION 3

DEVICE AND FAILURE MECHANISM CLASSIFICATION

Microelectronic device reliability depends primarily upon construction; process control, screening, qualification; and use characteristics. A review of the literature was performed to identify these characteristics which are listed in Table 3-1. The collected data was classified against these characteristics where possible. The classifications will be used to store data in the MICOM Storage Reliability Data Bank.

3.1 Device Construction

For convenience, device construction was broken into seven major areas: Bulk materiel and diffusion, oxide; metallization; glassivation; die bonding; chip connections; and packaging characteristics. Each of these areas identified in Figure 3-1 were analyzed for failure mechanisms which would be applicable in a missile's use environment from acceptance into the inventory to firing. Therefore, all important characteristics whether operational or storage dependent were included. Major device failure mechanisms are summarized in Table 3-2.

3.1.1 Bulk Materiel and Diffusion Characteristics

The primary reliability considerations in an operational environment associated with bulk phenomena are those which govern temperature of the device during operation. Devices are generally rated in terms of maximum allowable power dissipation. This power coupled with various thermal resistances and ambient temperature, determines the junction temperature of the device. Steps must be taken to maintain a controlled and uniform temperature since device degradation and failure modes, in most cases, are accelerated by increased temperature.

For most devices, the power requirements are not excessive and junction temperatures are controlled by using suitable heat-sink packages. For high-power devices, wafer design may include junction-temperature control considerations to prevent localized high currents and resultant "hot spot" formation.

Table 3-1. DEVICE CLASSIFICATION

CONSTRUCTION
- DIE PROPERTIES
- OXIDE
- METALLIZATION
- GLASSIVATION
- DIE BOND
- CHIP CONNECTION
- PACKAGE

DEVICE LEVEL PRODUCT ASSURANCE
- MIL-STD-883 QUALITY LEVEL
- SCREENS
- QUALITY CONFORMANCE INSPECTION
- PROCESS CONTROLS

ASSEMBLY AND SYSTEM LEVEL PRODUCT ASSURANCE TESTS

COMPLEXITY

LOGIC TYPE

USE ENVIRONMENT
- TRANSPORTATION AND HANDLING
- TEMPERATURE
- HUMIDITY
- STORAGE CONTAINER & LOCATION
- FIELD TEST DURATION & FREQUENCY
- DERATING

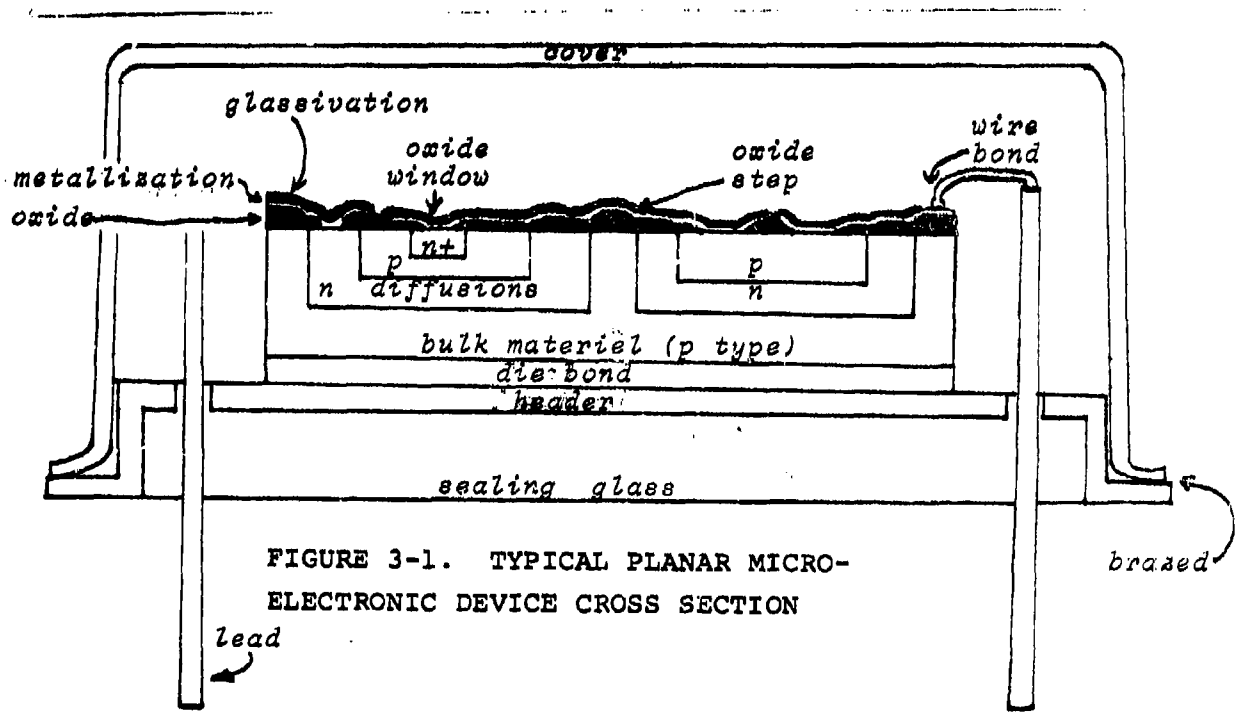

FIGURE 3-1. TYPICAL PLANAR MICRO-ELECTRONIC DEVICE CROSS SECTION

3.1.1.1 Bulk Defects

Bulk defects account for only a minor portion of the operational and storage failures. Primary areas of concern include dislocations (crystal lattice anomalies); impurity diffusions and precipitations; resistivity gradients; and cracks in the bulk materiel. These defects usually result during crystal preparation and are accelerated by mechanical, nuclear and thermal stresses.

The steep concentration gradients found in epitaxial diffusion result in crystal lattice strain which is subsequently released by the formation of dislocation structures. These structures contain edge components perpendicular to the concentration gradient. The chip is structurally weaker at the dislocation fault plane and failure can be triggered by mechanical stress.

Deviations in epitaxial growth, resulting in impurity diffusions, are another source of bulk failures. Impurity diffusion is more likely along edge dislocations, particularly along the arrays of edge dislocations that form small angles grain boundaries. The precipitation of impurities at the resulting crystal-lattice-orientation fault planes lowers the reverse breakdown voltage.

Resistivity gradients may be caused by a heat differential between the center and outer surface of the chip; by large local stresses caused by mechanical shock or vibration; and by neutron bombardment.

Cracks in the bulk silicon frequently result from thermal shock during processing. Although these defects are usually eliminated by normal quality control procedures, occasionally hidden cracks may either propagate to critical regions or result in breaks from additional shock or cycling.

The failure modes resulting from bulk defects include deviations in voltage breakdown and other electrical characteristics; secondary breakdown or uncontrolled p-n-p-n switching; or opens or shorts in the subsequent metallization.

3.1.1.2 Diffusion Defects

Diffusion defects account for approximately 5 to 15% of operational and storage failures. Other than those diffusion problems associated with bulk materiel defects, the primary area of concern is the diffusion process itself. These include mask alignment; contamination; mask defects; cracks in the oxide layer; and improper doping profiles. Diffusions that are due to misalignment of masks reduce the base and emitter or base and collector junction spacings. Other faults include discontinuous isolation diffusions and odd shapes or edges of diffusions. Diffusion defects are primarily accelerated to failure by thermal cycling and high temperature. Principle failure modes resulting from diffusion defects include deviations in device characteristics and shorts between the emitter and base.

3.1.2 Oxide Considerations

Junction passivation of silicon devices is generally accomplished by using thermally grown silicon dioxide (SiO_2). Other devices use phosphorous pentoxide (P_2O_5) over the SiO_2 layer. Beam Lead Sealed Junction (BLSJ) devices utilize a layer of silicon nitride (Si_3N_4) glass deposited over the grown SiO_2. Both P_2O_5 and Si_3N_4 overcoatings have been found to improve the surface stability of bipolar devices. These materials act as gettering agents for sodium ions, thus making the contamination far less mobile. The stability of the structural and electrical properties of the oxide play an important role in determining the electrical characteristics and reliability of the passivated device.

3.1.2.1 Oxide Defects

Oxide defects are significant contributors to digital device failures. Approximately 5 to 50% of operational failures are attributed to these defects. Current data on non-operating failures indicates that approximately 5 to 35% of storage failures are attributable to oxide defects. Primary areas of concern are pinholes, cracks, thin oxide areas, and oxide contamination.

Pinholes can be caused by faulty oxide growth, a damaged mask, poor photo resist or an undercut by the etching process. They vary in depth and in the worst case, expose the silicon to the metallized interconnections. Where the pinhole or metallization does not extend completely to the surface of the silicon, a time-dependent migration or low voltage breakdown mechanism may occur. Where the oxide is overcoated with a second layer, the frequency of pinhole defects decreases.

Oxide cracks occur as a result of the mismatch in the thermal expansion rate of silicon and silicon dioxide. Diffusion of metal to the silicon is then possible. Thin oxide and other oxide difficiencies cause electrical breakdown in the surface passivation from the metal conductor to component areas in the silicon. All of these defects lead to increased current leakages or shorts from the metallization to diffusion areas or substrate.

Ionic impurities in the oxide may cause inversion layers, channeling, and other related phenomena creating lower threshold voltage. Ionic contamination is generally a significant contributor to total oxide charge. The ions are usually mobile and, by drifting under the influence of an electric field, can cause appreciable device parameter instability. Silicon nitride has been shown to be an effective barrier to sodium migration. In Beam Lead Sealed Junction (BLSJ) devices, the silicon nitride seals the devices from sodium and since the platinum silicide and titanium metals also offer very low mobility to the alkaline ions, the BLSJ is inert to sodium.

Inversion and channeling phenomena occur only with an electric field present. Bipolar linear and MOS devices are affected by this phenomena greater than bipolar digital devices.

3.1.3 Metallization Considerations

A rather large number of metallization systems have been used on monolithic bipolar digital devices. The primary metals used have been aluminum, molybdenum-gold, and titanium-platinum-gold.

Aluminum is by far the most commonly used materiel for metallization. It is easily vacuum-evaporated and chemically etched, adheres well to the silicon and silicon dioxide and also forms a good ohmic contact to low resistivity silicon. Typically, a layer on the order of 1 micron thick is deposited by evaporation.

Gold is a better conductor than aluminum and is considerably more resistant to corrosion. However, it does not have sufficient adherence to silicon or glass surfaces to be used alone as a practical metallization system. Consequently, a two or three layer metallization system is required with the other material(s) forming an ohmic contact with the silicon. The gold adheres to the contact layer to form the conductor layer.

The molybdenum-gold metallization system is the one used most frequently.

The primary Beam Lead Sealed Junction process uses a platinum silicide to make the pre-ohmic contact. The next step is to deposit a layer of titanium metallization which provides contacts to the platinum silicide and silicon nitride. With this structure, gold will not diffuse to the junctions, but gold will not adequately bond to the titanium. Therefore, platinum is deposited on the titanium and then the gold is plated on to the platinum. Other multi-metal systems used include Platinum Silicide-Molybdenum-Gold; Platinum Silicide-Titanium-Palladium Gold; and Titanium Tungsten-Gold-Titanium Tungsten.

3.1.3.1 Metallization Defects

Failures related to metallization defects range from 7 to 26% in operational devices and current storage data indicates approximately 15% of the failures related to metallization.

3.1.3.1.1 Aluminum Metallization Systems

Aluminum metallization defects result from manufacturing deficiencies and also from mechanisms inherent to the metal system.

Processing deficiencies which subsequently result in device failures include thin metal layers, poor metal-to-oxide adhesion due to oil or other impurities on the wafer, undercutting of Al during etching of the metallization pattern, bridging of Al between conductors due to unremoved photoresist, smears and scratches in conductor stripes, misalignment of masks, insufficient deposition at oxide steps, oxide steps too steep, incomplete removal of oxide, etc.

These defects are accelerated to failure primarily by thermal stresses and result in open and shorted conductors.

Mechanisms inherent to the aluminum metal system include electromigration formation, aluminum silicon eutectic, and intermetallic compound formations with gold.

Electromigration, or current induced mass transport, is the movement of mass in a conductor when sufficient electric current is passed through the conductor. Since voids move through the conductor in a direction opposite to that of the mass transport, at a sufficient current density and/or temperature, a conductor will eventually open. Electromigration is currently a relatively minor reliability problem. The most direct way to eliminate electromigration is by design. The device power requirements and the interconnect cross-sectional area (including proper width-to-thickness ratios) should be balanced to keep maximum current density below 2×10^5 A/CM^2. Most of the actual device failures from electromigration in past years can be attributed to thin interconnect metallization due to lack of deposition-thickness control.

The aluminum-silicon eutectic formation (Kirkendall effect) creates a shift in the interfaces between the two alloys. The shift is due to a greater number of atoms from the silicon flowing to the aluminum than there are flowing in the reverse condition. The unbalanced flow rate causes voids under the metallization. This can cause seapration of aluminum from the die and eventual open circuit under mechanical stress.

Intermetallic compound formations can occur when gold wire is bonded to aluminum metallization. Some of the resulting compounds provide weak or brittle bonds or increased contact resistance. The Kirkendall effect further weakens the bond due to the formation of voids in the aluminum. Both room temperature and elevated temperature diffusions have been reported. Reliable gold-aluminum bonds can be made. It is necessary to minimize the total mass of aluminum available for diffusion and to keep to a minimum the cumulative time-temperature product experienced by the device in both manufacture and use.

3.1.3.1.2 Gold Metallization Systems

Many of the failure mechanisms observed in molybdenum-gold metallization systems can be attributed to processing problems. These include failures due to unsatisfactory adhesion of molybdenum to the silicon dioxide and of the gold layer to the molybdenum layer. These can be attributed to contamination of the surface and oxidation of the molybdenum layer prior to deposition of the gold. Other processing problems include: molybdenum undercutting during etching; scratches which expose the molybdenum to oxidation and subsequent opens, and corrosion of molybdenum from impurities introduced in the processing.

Gold-silicon eutectics can occur if pinholes exist in the molybdenum layer.

Failure mechanism data on Platinum Silicide-Titanium-Platinum-Gold metallization systems is just becoming available. Improved or eliminated failure modes include wire bond defects, alkali ion contamination, metallization corrosion, and aluminum migration. Possible failure mechanisms identified for these devices are all due to processing deficiencies. They include pinholes in the silicon nitride, thin silicon nitride, shorted metallization, platinum migration into the silicon, gold or titanium migration resulting from thin platinum, and contamination.

3.1.4 Glassivation Considerations

Both silicon nitride and phosphosilicate glass overcoatings have been found to greatly enhance the reliability of bipolar digital devices. These glassivation materiels act as gettering agents for sodium ions and when deposited over the total surface, including the metallization, the materiel provides an excellent protection against metallization scratches and loose particle shorts.

3.1.4.1 Glassivation Failure Mechanisms

Inversion and increased metal migration are two failure mechanisms that have been reported caused by glassivation. These new mechanisms are not fully understood but some causes have been postulated.

The induced inversion formation may result from some defects or contamination in the oxide layer which allow high fields to accumulate electronic charge over the underlying silicon. A poor interface between the oxide and glass then allows lateral charge movement along the interface. The lateral charge movement can induce inversion extensive enough to form a conducting channel which can cause device instability.

The increased metal migration is not as well understood but appears to be caused by the high pressure on the metal between the thermal and deposited glasses. Generally, the metal migration is associated with damage to the glass. Both aluminum and gold migration have occurred through the damaged glass to the adjacent conductor causing device failure.

A third possible failure mechanism has been discussed where condensation from any moisture in a package tends to contentrate on a crack in the glassivation, normally on the metal strips. This tends to increase the susceptibility for metal corrosion along the crack.

3.1.5. Die Bond Considerations

Die bonds provide mechanical support; in most cases, electrical contact; and also provide the principle path by which heat flows out of the silicon chip. Three techniques are in general use for attaching semiconductor devices to the

package substrate: alloy mount, frit mount and epoxy mount.

The alloy mount uses a thin layer of gold to form a eutectic alloy with the silicon and at the same time bond to the package substrate.

The frit mount uses a low-melting devitrifying glass in place of the gold.

The epoxy mount uses an epoxy cement to hold the semiconductor wafer to the substrate. Where an electrically conducting mount is needed, an epoxy filled with metal, usually silver, is used.

Beam Lead Sealed Junction devices do not use a die to header bond. Instead, the bonding of the beams provides the mechanical and thermal protection.

3.1.5.1 Die Bond Failure Mechanisms

Low strength chip-to-header bonds have been reported to result in approximately 2-7% of device failures, in both operational and storage environments.

The failure mechanisms include diffusion of the gold into the silicon producing void formations; brittle frit mounts resulting from impurities in the glass or improper firing cycles used for devitrification; mechanical stresses in epoxies where the temperature goes through the glass-transition temperature of the epoxy, and outgassing of organic materiel and separation of metal particles due to incomplete curing of the epoxy.

3.1.6 Chip Connection Considerations

Device connections are created by connecting wire leads to the device package, or through the use of beam lead or aluminum bump techniques. Wire bonding is accomplished primarily by thermcompression or by ultrasonic bonding techniques.

Thermocompression bonding required that the two materiels to be bonded be brought into intimate contact at an elevated temperature such that solid state diffusion can take place across the interface. The most widely used thermocompression bond is the bonding of gold wires, typically 1 mils in diameter,

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to aluminum bonding pads using ball bonds. Wedge bonds and stitch bonds are also used. Thermocompression bonding is also used to attach gold wires to molybdenum-gold metallization, for bonding beam lead devices; and for wedge bonding of aluminum wire to aluminum metallization.

The ultrasonic bonding technique is the most popular for attaching aluminum wire to aluminum metallization. In ultrasonic welding, two parts are bonded together through the simultaneous application of a clamping force that holds the two parts together and an ultrasonic vibrational force parallel to the place of the weld.

Both the gold and aluminum wires used for bonding must be hardened to facilitate handling during device assembly. Gold is work-hardened during wire drawing, then stressed relieved to a suitable tensile strength and elongation. Aluminum wire is hardened by additions of silicon and magnesium.

3.1.6.1 Bond Failure Mechanisms

Wire bond defects are reported to account for 15 to 45% of all device failures in an operational environment. Storage or non-operating data currently indicates from 19 to 76% of all device failures are bond related.

The principle failure mechanisms are process deficiencies including underbonding, overbonding, misaligned bonds, contaminated bonding pads or wire, and wire nicks, cuts or abrasions.

Thermocompression bonding of aluminum wires has a history of cracks at the heel of the bond, which later failed under power cycling.

The gold wire bonding to aluminum metallization has been a major concern in microelectronic devices. Intermetallic compound formations between these two metals combined with the formation of voids in the aluminum from the Kirkendall effect create high resistance or weakened and brittle bonds. Formation of the compounds and voids is accelerated by thermal

stresses. Design and processing criteria have been developed to minimize the occurrence of these formations. They include controlling the purity of the gold and providing thinner metallization at the bonding pad.

The aluminum wire bond to the gold header post has not been a significant contributor to device failures and is attributed to two factors: 1) the ratio of aluminum to gold is small, and 2) the bonds are not exposed to the same temperature as the gold wire to aluminum bonds on the chip during operation.

Failure mechanism data on beam lead sealed junction device bonding is limited. Processing deficiencies would be expected to be the primary problem, however, these are significantly reduced since the chip connection is made in the beam forming process which leaves only bonding of the beams to the header. All of the bonds of a single device are made simultaneously.

3.1.7 Package Considerations

Bipolar digital devices are packaged in a variety of materiels and configurations. These materiels include: metal, ceramic, glass, metal ceramic, epoxy, phenolic and other plastics. Package configurations include cans, flatpacks, inline and dual inline.

The main function of the package is to maintain a dry and inert atmosphere. Therefore, the primary reliability consideration is the hermetic seal of the package.

For metal-can packages, the seal is created by welding a nickel can or a nickel-plated steel can to a Kovar or steel header which is gold-plated. Glass is used to seal the package at the electrical leads and to isolate these leads from themselves and the header.

Ceramic package seals are formed by glass, brazed moly-manganese metallization or so-called "solder glasses."

The plastic package, formed by molding the semiconductor device in molten plastic, is not a hermetic package. Plastics used are, for the most part, epoxy materials.

TABLE 3-2. MONOLITHIC DEVICE FAILURE MECHANISMS

FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
BULK DEFECTS				
Dislocation and Stacking Faults	Lattice strain due to steep concentration gradients finally released as dislocations.	Mechanical Stress Hi Temp	Degradation of junction characteristics.	Electrical Test
Impurity Diffusions and Precipatations	Diffusions along dislocations during epitaxial growth.	Hi Temp Power Burn-in Thermal Cycling	Low reverse breakdown voltage.	Electrical Test
Resistivity Gradiants	Large local stresses.	Mechanical Shock Vibration Nuetron Bombardment	Change in component values.	Electrical Test
Cracks in Bulk Materiel	Thermal shock during processing.	Mechanical Shock Thermal Cycling Hi Temp	Opens or Shorts in metal. Junction degradation.	Precap Visual Electrical Test

TABLE 3-2. MONOLITHIC DEVICE FAILURE MECHANISMS

FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
DIFFUSION DEFECTS				
Improper Diffusions	1) Faulty Mask Alignment 2) Dust or other Contaminants on mask 3) Defects in mask itself 4) Cracks in oxide	Hi Temp Thermal Cycling	Shorts Opens Changes in Device Characteristics.	Precap Visual Electrical Test
Improper Doping Profile	Process control problem.	Thermal Cycling Hi Temp. Storage	Unstable Components	Electrical Test
OXIDE DEFECTS				
Inversion Layer Phenomena	1) Thermal oxidation of Silicon producing n or p type surface. 2) Charged impurities.	Hi Temp. Power Burn-in Reverse Bias	Emitter to Collector Short Lower Threshold Voltage	Electrical Test
Pinhole	Faulty Oxide Growth due to: 1) Dust particles or other contaminants. 2) Minute mask flaws. 3) Etch undercut.	Hi Temp. Thermal Cycling Power Burn-in	Short	Electrical Test

TABLE 3-2. MONOLITHIC DEVICE FAILURE MECHANISMS

FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
OXIDE DEFECTS -	CONTINUED			
Cracks	Mismatch in Thermal Expansion rate.	Hi. Temp.	Short	Electrical Test
Thin Oxide	Improper Process Control.	Hi. Temp.	Short	Electrical Test
METALLIZATION DEFECTS				
Surface Flaws	Scratched or smeared metallization during processing.	Thermal Cycling	Open Short	Precap Visual Electrical Test
Insufficient Coverage at Oxide step	1) Misalignment of masks. 2) Insufficient deposition at oxide steps. 3) Oxide step too steep. 4) Oversintering of metal to silicon. 5) Incomplete removal of oxide.	Hi. Temp. Thermal Cycling Power Burn-in	Open Hi Resistance Connections	Precap Visual Electrical Test
Under etched Metallization	Improper Etching.	Hi. Temp. Thermal Cycling Power Burn-in	Short	Precap Visual Electrical Test

TABLE 3-2. MONOLITHIC DEVICE FAILURE MECHANISMS

FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
METALLIZATION DEFECTS - CONTINUED				
Voids under Metallization	1) Overetching causing undercutting of metallization. 2) Kirkendall effect of disimilar alloys.	Hi. Temp. Thermal Cycling Mechanical Stress	Open	Precap Visual Electrical Test
Non-adhesion of Metallization	1) Contamination of surface. 2) Improper alloying temp. or time.	Hi. Temp. Thermal Cycling	Open	Precap Visual Electrical Test
Metal Migration (Hillocks, Voids, Whiskers, etc.)	Insufficient metal thickness, Scratches, grain size, etc.	Hi. Temp. & Current Density	Open Short Current Leakage	Precap Visual Electrical Test
Increased Resistance of Metallization	Thickness of oxide.	Hi. Temp.	Out of Tolerance	Electrical Test
GLASSIVATION DEFECTS				
Inversion Phenomenon	Poor Interface between oxide layer & glassivation layer.	Hi. Temp. & Reverse Bias	Out of Tolerance	Electrical Test

TABLE 3-2. MONOLITHIC DEVICE FAILURE MECHANISMS

FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
GLASSIVATION DEFECTS - CONTINUED				
Metal Migration	Damaged Glass - Pressure Between oxide & glassivation layers.	Hi. Temp. & Current Density	Open Short Current Leakage	Electrical Test
Oxide Cracks Corrosion	Thermal Shock During Processing.	Temp. Cycling	Open	Precap Visual Electrical Test
DIE BONDING DEFECTS				
Voids between header & die	Incomplete coverage of bonding materiel.	Hi. Temp. Vibration Shock	Open	Precap Visual Electrical Test
Cracked or lifted die to header bond.	1) Weak metal eutectic bond due to oxide on reverse side of silicon. 2) Glass frit facture in flexible package.	Acceleration Shock Vibration Hi. Temp.	Open	Precap Visual Electrical Test

TABLE 3-2. MONOLITHIC DEVICE FAILURE MECHANISMS

FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
DIE BONDING DEFECTS - CONTINUED				
Cracked Silicon Die	Strains during die attach.	Acceleration Shock Vibration	Open	Precap Visual Electrical Test
WIRE BONDING DEFECTS				
Separation of Bond	1) Underbonding. 2) Contamination of Bonding. 3) Cracks in bond due to overbonding.	Hi. Temp. Shock Vibration	Open	Precap Visual Electrical Test
Bond Shorts	1) Overbonding. 2) Insufficient bonding pad area or spacing. 3) Improper bond alignment.	Hi. Temp. Power Burn-in Vibration Shock Thermal Cycling	Short	Precap Visual Electrical Test
Broken wires & Reduced wire size.	1) Overbonding. 2) Nicks, cuts or abrasions in wire during processing.	Hi. Temp. Shock Vibration	Open	Precap Visual Electrical Test

TABLE 3-2. MONOLITHIC DEVICE FAILURE MECHANISMS

FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
WIRE BONDING DEFECTS - CONTINUED				
Wire Shorts.	Unremoved pigtails.	Hi. Temp. Shock Vibration	Short Intermittent Shorts	Precap Visual Electrical Test
Intermetallic Compound Formation	Various Time-Dependent Formations of a Chemical Compound at metal-metal contacts: 1) Purple Plague $AuAl_2$. 2) Black Plague Au-Si-Al. 3) White Plague - Aluminum Hydroxide. 4) Silver Plague - Tin Migration. 5) Red Plague - Copper Oxide on Silver Plate over Copper.	Hi. Temp. Power Burn-in Thermal Cycling	Open	Precap Visual Electrical Test
FINAL SEAL DEFECTS				
Poor Hermetic Seal	Fractured Glass or Imcomplete Weld, Braze, etc.	Thermal & Mechanical Stress	Corrosion Causing Opens, Shorts or Performance Degration.	Leak Tests

TABLE 3-2. MONOLITHIC DEVICE FAILURE MECHANISMS

FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
FINAL SEAL DEFECTS - CONTINUED				
Fractured Package	Improper Handling or Improper Seal Leak Test	Thermal & Mechanical Stress	Corrosion Causing Opens, Shorts or Performance Degration	Visual
Internal Wires Shorted to Conductive Lids or chip periphery	Slack in leads.	Mechanical Stress Temp. Cycling	Short	Radiographic Electrical Test
Current Leakage Between Leads	Low Resistance Leak due to Reduction of P_bO Glass to P_b.	Hi. Temp.	Current Leakage	Electrical Test
Broken or Bent External Leads	Improper Brazing or Handling	Hi. Temp. Mechanical Stress	Open	Visual Lead Fatigue Tests
Improper Marking	Process Control Problem		Not Operative	Electrical Tests

TABLE 3-2. MONOLITHIC DEVICE FAILURE MECHANISMS

FAILURE MECHANISM	CAUSE	ACCELERATING ENVIRONMENT	FAILURE MODE	DETECTION METHOD
CONTAMINATION				
Surface, Wire or Bond Corrosion	Corrosive Residue & Moisture such as: 1) Photo Resist 2) Chlorine in wire Lubricant 3) Etch pits in oxide, trapping sodium or other corrosive agents 4) Outgassing from organic materiels. 5) Weld glasses 6) Incorrect atmosphere sealed in package 7) Loss of package hermiticity	Hi. Temp. Storage	Open Short Degraded Operation	Electrical Tests
Conductive Particles in Package	1) Solder particles 2) Wire particles 3) Flaking metallization 4) Die particles 5) Die bond materiel particles	Vibration Shock Thermal Cycling	Short	Electrical Tests
Corrosion at Glass Ceramic Interface	Small lead materiel junction at interface exposed to environment after lead plating.	Hi. Temp. Storage	Open	Visual Electrical Tests

3.1.7.1 Package and Lead Failure Mechanisms

Device failures attributed to package defects have been reported from 8 to 28% of operational failures. In many cases of failure reports, the resulting contamination and corrosion is reported and not the seal defect. Special test programs on devices have shown hermeticity problems to be substantial.

Failure mechanisms besides the seal leaks are fractured packages due to improper handling, loose solder balls formed in sealing the package which later short conductors, current leakage between leads from formation of lead from lead oxide in the glass, broken or burnt external leads and improper marking. All of these are process defects.

3.1.8 Linear Device Characteristics

Certain construction characteristics and resulting failure mechanisms described for the digital devices exhibit a greater degradation on linear devices and therefore are briefly discussed below.

Most digital device families utilize components on the chip in a saturated switching mode. This allows the various components to have wide ranges of values and undergo considerable drift and still maintain proper circuit operation. The linear circuit however, is much more sensitive to variations in individual component characteristics. The linear device usually requires operation of all transistors in the active region and may have a high voltage gain. Both of these factors mean that any slight drift in the various component parameters especially in the input stage can result in out of tolerance failure modes.

Although this instability can result from a number of causes, the primary failure mechanisms are surface related problems. They include ionic contamination and defects in passivation, metallization and glassivation layers.

The contamination most often reported as the cause of inversion has been the sodium ion. This positively charged ion is extremely mobile in the usual silicon dioxide passivation and quickly moves close to the silicon where it can easily induce an inversion. Because of its positive charge sodium is responsible for the inversion of p-type materiel, inverting the bases of normal NPN integrated transistors and causing failure. Bias changes can redistribute the positive ion concentration resulting in unstable device electrical characteristics.

Doping the silicon dioxide with phosphorous or depositing a phosphorous doped glass over the thermal silicon dioxide has been used to decrease the mobility of the sodium ion. Silicon nitride layers are also being used for the same purpose.

Defects such as cracks and crazing of passivation and glassivation layers have also been reported to result in the inversion phenomenon.

In all of these cases, the inversion layers or channels are created with an applied bias. Once bias is removed, the ion contaminants or surface inversion layers tend to disperse. It has been reported that devices exhibiting these inversion characteristics have been missed in the reverse bias screen and go undetected until operation. This occurs when bias is removed before the devices are cooled down or the parameter tests are performed a considerable period after the bias has been removed. In each of these cases, the inversion phenomenon has disappeared.

For the storage environment, the inversion phenomenon could only be generated if the devices were contaminated by some external source, or a defect in a phosphorous doped layer or silicon nitride layer allowed ionic contaminants to concentrate in a single area. Once this occurred a certain amount of operating time (typically 1 hour up to 1 day) would be required for the inversion to form. For highly contaminated devices, several minutes may be all that is required. Generally, in the missile application, operating times are short and the inversion phenomenon has not been reported as a major problem in the field data.

3.2 Long Term (20 year) Failure Mechanism Analysis

The data analyzed in this report is on devices stored for up to nine years. A separate study has been conducted on microelectronic failure mechanisms for up to twenty years storage time by the Georgia Institute of Technology. This report, prepared for the U. S. Army Missile Research and Development Command, considers physical and chemical properties of the electronic devices and the environments in which a device may be subjected from processing through twenty years of field storage. Conclusions from this report concerning bipolar devices are contained below. For details, the reader is referred to Report DD14-23, "Reliability Factors for Electronic Components in a Storage Environment," by B. R. Livesay and E. J. Scheibner, Applied Sciences Laboratory, Engineering Experiment Station, Georgia Institute of Technology, September, 1977.

1. The most important environmental forcing functions, or stresses, in storage are mechanical, chemical and low thermal. Mechanical stresses occur due to thermal-mechanical interactions and residual stresses. Chemical stresses result from contaminants such as residual process chemicals and environmental gases which are introduced through improper or failed seals. Although purely thermal stresses have much less importance in storage than operating environments, certain low temperature reaction rates and diffusion processes are temperature dependent.

2. The synergism of the three primary storage stresses is critical. Any one of the three acting alone may not be particularly damaging but the combined effect of two or three forcing functions acting together is likely to cause device failures.

3. Environmental extremes for Army missiles in storage have involved temperatures of -50°C to +75°C, diurnal cycling of 70°C, 100 percent relative humidity, direct sea spray, industrial pollutants, some mechanical shock and fungus.

4. The failure mechanisms of greatest importance in storage have been identified as those related to various marginal manufacturing mistakes, corrosion processes and mechanical fracture. Electrical or potential current induced degradation processes should not be important in the storage environment. Moisture within a package is probably the most important factor for both corrosion and mechanically induced failures in storage. Chemicals including moisture trapped within a package due to improper cleaning or because of evolution from materials such as polymers are a critical concern for long-term reliability. The package seal is also critical for keeping out atmospheric contaminants. Thermal-mechanical stresses aided by chemical agents will cause crack propagation in seals, passivation layers, bonds, metallization layers and the silicon chip.

5. New manufacturing methods such as the Tape Automated Bonding technology should be continually evaluated to determine if there are potential storage failure mechanisms. For example, are there detrimental effects in a storage environment from probable impurities introduced during bump plating and bonding operations?

6. The presence of defects such as impurities, dislocations, microcracks, interfacial faults and grain boundaries in the materials of a microcircuit structure can result in failure due to low temperature atomic diffusion processes.

7. Particulate matter is one of the dominant concerns as a storage failure mechanism.

8. The hermeticity of microelectronic packages is an important concern for long-term storage conditions. The screen tests for determining the effectiveness or hermeticity of the package seals includes a fine leak rate test. The maximum allowable leak rate specified for this test should be lowered to 10^{-10} atm cm^3 sec^{-1} for devices that are expected to be stored because of the exchange of gases between the initial package ambient and the external storage environment for packages with a finite size leak.

9. All microcircuit packages should be vacuum bakes at 150°C for at least 4 hours and sealed in dry nitrogen without ever being exposed to moisture containing gases such as air. The moisture content of the nitrogen sealing chamber should be less than 100 ppm.

10. Significant improvements are needed in the measurement technology for moisture and other gases in microcircuit packages. Current methods are too expensive and complicated while providing insufficient sensitivity and wide variations in numerical values for supposedly identical gas contents.

11. The use of plastics introduces high risks of differential expansion problems which result in mechanical damage such as pulling apart leads.

12. Missiles placed in storage should never contain electronic parts employing polymers for package seals. Polymers will transmit moisture and other gases.

13. Screening and accelerated testing procedures of Army missiles must have steps determined by potential storage failure porcesses. There is doubt that the screening sequence contained in MIL-STD-883A is fully appropriate to the storage environment.

14. There is widespread controversy about the optimum number of cycles in a temperature cycling screen test. Opinions vary from 25-300 cycles for effective screening but the use of only 10 cycles is not considered to be of any value. Results of the Rockwell International screen test program have not resolved this question.

15. Thermal shock should never be used as a screen test stress for hermetic devices placed in stored missile systems.

16. The metallurgical consequences of an upper limit of 150° vs. 125°C for temperature cycling and stabilization bakes with regard to solders should be investigated.

17. The philosophy necessary for developing meaningful screen testing parameters is to concentrate on determining the stress-duration levels required to reveal well defined device faults. The capability is therefore needed for fabricating devices with deliberate defects of desired type, severity and number.

18. Only general environmental data are currently available for the temperature, environmental gases, vibration, etc. expected in storage. There is need for specific information concerning the interior of a missile in storage in order to make judgments concerning future reliability factors. The chemical factors associated with moisture, evolved gases and fungus need to be developed at four levels:

1. Within the storage structure (igloo, shed, etc.)
2. Within the missile container
3. Within the missile electronic system compartment
4. Within individual component packages

A measurement program should be established so that actual data will be available concerning these factors.

19. The effectiveness of desiccant materials used within Army missiles should be evaluated. This topic was not pursued during this program but questions were raised by several organizations.

20. The various types of missile storage containers should be evaluated to determine how well they protect missiles from storage environments most critical to the electronic systems.

21. Procedures should be in effect to close the loop concerning the detailed analysis of parts failing in service and manufacturing parameters. Failures in field environments are generally more severe than indicated by initial predictions. Feed-back from service failures should be available to guide design decisions of future systems.

22. Measurements of permeabilities, diffusion coefficients, and solubilities of water in representative polymers should be made so that good data are available and effects of temperature, pressure, mechanical strain, previous sorption, and synergism of two or more penetrants be understood. Data of thermal expansion, glass transitions, and viscoelastic responses of polymer encapsulants and adhesives are too meager for design of circuit systems. Measurements are needed here.

23. Age sensitive materials used in missile systems must be well characterized. Missile storage reliability is determined by the stability of the materials used to fabricate individual parts within the system while exposed to the storage environment of a tactical missile. There is a strong need for compiling material degradation data from the technical literature, directed experiments and theoretical calculations.

3.3 Device Level Product Assurance

The manufacturing controls and procurement methods for military equipment are normally determined by the criticality of the device in the system and the uniqueness of the device. Procurement specifications determine, to a significant degree, the reliability of the device in the field.

For standard devices in high volume production with established reliability, the parts may be procured according to the specifications in MIL-STD-883 and MIL-M-38510 or equivalent manufacturer specifications. The three quality levels defined in the military specifications are:

Class "A" - Devices intended for use where maintenance and replacement are extremely difficult or impossible, and reliability is imperative.

Class "B" - Devices intended for use where maintenance and replacement can be performed, but are difficult and expensive, and where reliability is imperative.

Class "C" - Devices intended for use where maintenance and replacement can be readily accomplished and down time is not a critical factor.

A Class "D" level has also been defined in this report to identify the manufacturer's commercial quality level.

In the procurement of standard and non-standard devices, a second method is to use specific user specifications. The user specifications are generally closely related to the military specifications but tailored for the specific use requirements.

A third method in use is the procurement of devices according to a particular quality level (MIL-STD-883, MIL-M-38510, and/or user specification) and the performance of additional qualification and screening at the system contractors, subcontractors or government facilities.

The so called "captive line" is being used as a fourth method of procuring high reliability parts. In this case, the devices are built to the user's specifications and no

part of the qualified process and line can be changed without approval of the procuring organization.

All of these techniques require some form of manufacturing, quality conformance certification and may include procuring organization periodic inspection or continuous monitoring of the production lines.

3.3.1 Process Controls

Various combinations of process control techniques are used on manufacturing lines. The techniques may include in-process lot acceptance, process monitoring, process audit/surveillance, and operator certification.

In process lot acceptance is a sampling test, made to a specific acceptable quality level (AQL). It is used especially in high throughput points, such as those in the early stages of device manufacturing.

Process monitoring keeps track of variables such as bonding temperature, gas flow rates, furnace temperature, and rinse times. Process monitoring may also be used to measure operator performance and to insure product control where in-process lot acceptance is not performed.

Audits and general surveillance of both the process and the product may be performed at regular intervals to assure adherence to the manufacturing specifications.

For operator certification, production operators and inspectors may be regularly graded and classified. In this case, the work of the best operators is subject to no inspection or a minimum amount of inspection. The work of the next best operator is sample-tested and for the poorest operator's work, 100 percent testing may be performed.

Typical process points where these types of controls may be instituted are contained in Table 3-3.

3.3.2 Device Level Product Assurance

The decision on the amount of product qualification and screening to be performed is dependent on the quality and reliability requirements of the application. A second

TABLE 3-3. PROCESS CONTROL POINTS

MATERIAL PROCESSING

STARTING SLICE CONTROLS
ORIENTATION, RESISTIVITY, THICKNESS, BOW, TAPER

MECHANICAL POLISH CONTROLS
THICKNESS, TAPER, SURFACE FINISH, DISLOCATIONS

OXIDATION CONTROLS
THICKNESS, PINHOLES, CLEANLINESS

EPITAXIAL DEPOSITION CONTROLS
THICKNESS, RESISTIVITY, STACKING FAULTS

PHOTORESIST CONTROLS
DIMENSION, ALIGNMENT, ETCH COMPLETENESS

DIFFUSION CONTROLS
FURNACE CONTROL, DIFFUSION DEPTH, RESISTIVITY, ELECTRICAL TESTS

METALLIZATION
EVAPORATOR CONTROL, THICKNESS ADHERENCE, PATTERN DEFINITION, SEM EXAMINATION

BACK GRIND OF SLICE
GRINDER CONTROL, THICKNESS, CONTAMINATION

BAR INSPECT LOT ACCEPTANCE
PROBE AND SCRIBE DAMAGE, PEELING METAL, CRACKS

ASSEMBLY

HEADER INSPECTION
BONDABILITY, DISCOLORATION

ALLOY MOUNT
ALLOY COMPLETENESS, BAR ORIENTATION, PARTICLES, ADHERENCE

BONDING
MACHINE CONTROL, BOND STRENGTH, WORKMANSHIP

PRE-CAP LOT ACCEPTANCE

WELDER CONTROL
PARTICLES, MOISTURE LEVELS

HERMETICITY

determining factor is the life cycle cost trade-off of detecting defects at the part level versus detecting them at the board or module level during assembly versus detecting them in the system field use.

MIL-STD-883 and MIL-M-38510 primarily control the military part level product assurance requirements. The requirements include manufacturer certification, qualification inspection, quality lot conformance inspection and screening.

3.3.2.1 Qualification Certification

In the specifications, the microcircuit manufacturer is required to have his product assurance program certified for each quality level: A, B, and C. For Class A devices, manufacturer line certification is also required.

3.3.2.2 Qualification Inspection

A certified manufacturer must qualify individual device types or groups of related devices by subjecting them to, and demonstrating that, they satisfy all the groups A, B, and C requirements for the specified device class and type of microcircuits. This qualification inspection must be repeated at intervals no greater than three months unless otherwise specified.

3.3.2.3 Quality Lot Conformance Inspection

Quality lot conformance inspection is required by the military specifications for all three quality levels. Samples from each lot are drawn and electrical and environmental tests performed on subgroups of the sample. The sample size and number of failures allowed in the tests are determined statistically from the size of the lot and the required reliability. In the statistical analysis, the required reliability is converted into a factor denoting the lot tolerance percent defective (LTPD). The number of failures allowed in the tests is based on the sample size and the LTPD for that test. The lot is accepted if the observed number of defectives is equal to or less than the preselected acceptance number for the sample size. Specific tests required are summarized in Table 3-4.

The group A tests include static, dynamic, functional and switching parameter electrical testing. All devices used in the group A tests that comply with the requirements may be returned to the lot.

The group B tests assess the physical, bond and lead strength of the devices. The group B tests are considered destructive and all devices used in these tests must be removed from the lot.

The group C tests are environmental tests which subject the devices to environmental extremes in order to detect weak devices or drifting parameters. The thermal, mechanical and salt atmosphere tests are considered destructive and devices used in these tests must be removed from the lot. All devices in the High Temperature Storage, Operating Life and Steady State Reverse Bias Tests that comply with the requirements may be returned to the lot.

As indicated in Table 3-4, the primary distinction in quality levels for conformance testing is the number of defectives allowed in the sample. Also for Class A devices, operating life tests and steady state reverse bias tests are required.

3.3.2.4 Screening

The screening or testing of 100 percent of the devices varies among programs. The primary concern of screening is is to weed out the weak devices without creating defects or weaknesses in good devices. MIL-STD-883 specifies the screen type and method to be used but generally leaves the severity of the screen up to the procuring organization to fit the use requirements. As stated previously, users may modify the required screens by the vendor, or may perform additional screens at his own facilities. Table 3-5 summarizes the basic screening procedures specified in MIL-STD-883.

The principle differences in screening for Class A, B and C devices are indicated in Table 3-5.

TABLE 3-4. QUALITY CONFORMANCE TESTING

GROUP A TESTS

TEST	CONDITION	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 1 Static Tests at 25°C.	Per applicable procurement document.	5	5	5
Subgroup 2 Static Tests at max. rated operating temp.		5	7	10
Subgroup 3 Static Tests at min. rated operating temp.		5	7	10
Subgroup 4 Dynamic Tests at 25°C.		5	5	5
Subgroup 5 Dynamic Tests at min. operating temp.		5	7	10
Subgroup 6 Dynamic Tests at min. operating temp.		5	7	10
Subgroup 7 Functional Tests at 25°C.		3	5	5
Subgroup 8 Functional Tests at max. & min. rated operating temp.		5	10	15
Subgroup 9 Switching Parameter Tests at 25°C.		5	7	10
Subgroup 10 Switching Parameter Tests at max. rated operating temp.		5	10	15
Subgroup 11 Switching parameter Tests at min. rated operating temp.		5	10	15

TABLE 3-4. QUALITY CONFORMANCE TESTING

GROUP B TESTS

TEST	CONDITION	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 1 Physical Dimensions	External	10	15	20
Subgroup 2 a. Marking Permanancy		4 devices (no failures)		
b. Visual & Mechanical	Internal & External	1 device (no failures)		
c. Bond Strength 1.Thermocompression	Bond Sheer or Wire Pull	5	15	20
2.Ultrasonic or Wedge	Bond Sheer or Wire Pull			
3.Flip Chip	Bond Sheer			
4.Beam Lead	Bond Sheer or Bond Pull			
Subgroup 3 Solderability	Soldering Temp of 260±10°C.	10	15	15
Subgroup 4 Lead Fatigue	3 bending cycles through a 90° arc.	10	15	15
Seal a. Fine b. Gross				
GROUP C TESTS				
Subgroup 1 Thermal Shock	15 cycles min. at -55°C to 125°C.	10	15	15
Temperature Cycling	-65°C to 150°C (cycles as specified)			
Moisture Resistance				
Seal a. Fine b. Gross				
End Point Electrical Parameters	per applicable procurement document.			

TABLE 3-4. QUALITY CONFORMANCE TESTING

GROUP C TESTS (CONTINUED)

TESTS	CONDITION	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 2		10	15	15
Mechanical Shock	5 pulses at 1500 G level			
Vibration, variable Frequency	20-200Hz, 20G acceleration, 16 minutes min. in each plane.			
Constant Acceleration	30,000 G level.			
Seal				
a. Fine				
b. Gross				
End Point Electrical Parameters	per applicable procurement document.			
Subgroup 3		10	15	15
Salt Atmosphere	24 hours at 35°C.			
Subgroup 4		7	7	7
High Temperature Storage	150^{+50}_{-25}°C Storage, 1000 hours.			
End Point Electrical Parameters	per applicable procurement document.			
Subgroup 5				
Operating Life Test	1000 hours per applicable procurement document	7	--	--
End Point Electrical Parameters				
Subgroup 6				
Steady State Reverse Bias	72 hours at 150°C per applicable procurement document.	7	--	--
End Point Electrical Parameters				

The internal visual (precap) test checks the internal physical construction, marking and workmanship before capping the device.

Class A devices are examined for metallization scratches, voids, corrosion, bridged interconnections, misalignment and incomplete window coverage, oxide defects, incomplete junction coverage, improper contact cuts, and chipped oxide between the bond or metallization periphery and the edge of the chip, diffusion faults, foreign materiel, incorrect bond size or location, damaged wires, incorrect wire length, extra wire materiel, insufficient distance between wires, improper chip orientation, and package defects.

The Class B device internal visual requirements are less stringent and include examination for metallization scratches, voids and bridged interconnections, chipped oxide between bond or metallization periphery and the edge of the chip, foreign material, incorrect bond location, incorrect wire tension, cracked die and improper chip orientation.

No Class C internal visual is required for monolithic devices.

The stabilization bake temperature cycling and seal tests are the same for all quality levels. Recommended temperature extremes of exposure for specific metallization systems are -65°C to 200°C for aluminum/aluminum systems; -65°C to 150°C for gold/aluminum systems; and -65°C to 300°C for gold/gold systems.

Thermal shock, mechanical shock, reverse bias burn-in, and radiographic inspections are required for Class A devices only.

The constant acceleration test stresses two planes of the Class A devices while only one plane of the Classes B and C.

Burn-in tests of 240 hours for Class A devices and 168 hours for Class B devices are required. No burn-in is required for Class C.

TABLE 3-5. MIL-STD-883 SCREENING
PROCEDURE SUMMARY (Method 5004)

SCREEN	CONDITION	SCREEN SAMPLE		
		CLASS A	CLASS B	CLASS C
Internal Visual (Precap)	See text for Class A, B & C.	100%	100%	100%
Stabilization Bake	24 hours minimum at 75°C minium.	100%	100%	100%
Thermal Shock	15 cycles minimum at -0 to 100°C minimum.	100%	---	---
Temperature Cycling	-65° to 150°C min. Cycles as specified.	100%	100%	100%
Mechanical Shock	20,000 G level (peak) one pulse shock in y_1 plane only or 5 shock pulses at 1500 G level (peak) in Y_2 plane.	100%	---	---
Constant Acceleration	30,000 G level in Y_2 plane, then Y_1 plane for Class A. Y_1 plane only for Classes B & C.	100%	100%	100%
Seal a. Fine b. Gross		100%	100%	100%
Interim Electrical Parameters	Per applicable procurement document.	100%	---	---
Burn-in Test	240 hours at 125°C (Cl.A) 168 hours at 125°C (Cl.B)	100%	100%	---
Interim Electrical Parameters	Per applicable procurement document. (test required only when reverse bias burn-in is used)	100%	---	---
Reverse Bias Burn-in	72 hours at 150°C min. (when specified for MOS or linear devices).	100%	---	---
Final Electrical Tests				
a.Static 25°C	Per applicable procurement document.	100%	100%	100%
max/min Temp		100%	100%	---
b.Dynamic		100%	100%	---
c.Functional		100%	100%	100%
Radiographic		100%	---	---
External Visual		100%	100%	100%

The Class A and B final electrical tests include static, dynamic and functional tests at 25°C with static tests at maximum and minimum rated operating temperatures also. The Class C final electrical tests require only static and functional tests at 25°C.

3.3.2.5 Device Level Product Assurance Classification

The primary product assurance classifications which effect the device reliability are the MIL-STD-883 quality levels: Class A, B and C plus the commercial quality level designated as Class D. Quality conformance inspections and screens over and above these levels are used to also identify the quality level. Special considerations such as captive lines are further used to classify the quality level.

3.4 Module, Assembly and System Level Product Assurance

Additional screens and qualification tests performed at the module, assembly and system level also effect the device reliability in its use environment. Typically a major item may be subjected to operating times at high and low temperatures, shock, and vibration. For purpose of classifying the devices for reliability, such screens are identified where data is available.

3.5 Device Function and Complexity Classification

Bipolar digital devices consist of various logic families developed over the years with certain new types virtually replacing older ones. The complexity of the device which has generally increased during the years depends on the use function.

RTL or resistor-transistor logic is one of the earliest types of logic and its use is declining due to increased use of later developed circuits. Its immunity to external noise is less than the newer families.

DTL or diode transistor logic use is also declining in new system design. It features noise immunity and has moderate speed.

TTL or transistor-transistor logic is much faster than

DTL. More complex functions are available in this family than in any of the logic families. Its immunity to external noise is very good.

A special type of TTL called Schottkey TTL operates at faster speeds.

ECL or emitter-coupled logic has a very high logic speed. Transistors are not allowed to saturate and switching is performed at relatively constant current.

Other logic types include: CTL (complementary-transistor logic); RCTL (Resistor-capacitor-transistor logic); DCTL (direct coupled transistor logic); and CML (current-mode logic).

The main complexity classifications are small scale integration (SSI) which includes devices with up to 11 gates; mdeium scale integration (MSI) which includes devices with from 11 to 99 gates; and large scale integration (LSI) which includes devices with over 100 gates.

Table 3-6 presents a sample of some digital functions and their complexities.

TABLE 3-6. DIGITAL MICROCIRCUIT COMPLEXITY

COMPLEXITY	FUNCTION	COMPLEXITY	FUNCTION
SSI (up to 5 gates)	Simple Gate Dual Gate Simple Buffer Dual Buffer Simple Expander Dual Inverter	MSI (12 to 99 gates)	JK Flip Flop Dual Exclusive OR One Shot Multivibrator JK/RS Flip Flop Dual Simple Flip Flop RS Flip Flop/Converter Ripple Converters Dual JK Flip Flop
SSI (6 to 11 gates)	Triple Gate Quad Gate Exclusive OR Gate Adder Dual Expander Triple Expander Quad Inverter Driver Hex Inverter Simple Flip Flop Pulse Exclusive OR		

Bipolar linear devices consist of various functions. The complexity of the device depends on the use function.

The main complexity classifications are small scale integration (SSI) which includes devices with up to 44 transistors; medium scale integration (MSI) which includes devices with from 45 to 400 transistors; and large scale integration (LSI) which includes devices with over 400 transistors.

Table 3-7 presents a sample of some linear functions and their general complexity levels.

TABLE 3-7. LINEAR MICROCIRCUIT COMPLEXITY

COMPLEXITY	FUNCTION
SSI (up to 20 transistors)	IF Amplifier Dual Differential Amplifier Volt Regulator Differential Amplifier RF Amplifier Line Driver Video Amplifier Dual-line Receiver Power Amplifier
SSI (20 to 44 transistors)	Operational Amplifier Voltage Comparator Dual Voltage Comparator D. C. Amplifier Demodulator

3.6 Use Environment

A missile system may be subjected to various modes of transportation and handling, temperature soaks, climatic extremes, and activated test time and "launch ready" time in addition to a controlled storage environment. Some studies have been performed on missile systems to measure these environments. A summary of several studies is presented in report BR-7811, "The Environmental Conditions Experienced By Rockets and Missiles in Storage, Transit and Operations" prepared by the Raytheon Company, dated December 1973.

In this report, skin temperatures of missiles in containers were recorded in dump (or open) storage at a maximum of 165°F (74°C) and a minimum of -44°F (-42°C). In non-earth covered bunkers temperatures have been measured at a maximum of 116°F (47°C) to a minimum of -31°F (-35°C). In earth covered bunkers, temperatures have been measured at a maximum of 103°F (39°C) to a minimum of 23°F (-5°C).

Acceleration extremes during transportation have been measured for truck, rail, aircraft and ship transportation. Up to 7 G's at 300 hertz have been measured on trucks; 1 G at 300 hertz by rail; 7 G's at 1100 hertz on aircraft; and 1 G at 70 hertz on shipboard.

Maximum shock stresses for truck transportation have been measured at 10 G's and by rail at 300 G's.

Although field data does not record these levels, where available, the type and approximate character of storage and transportation are identified and used to classify the devices.

SECTION 4

STORAGE DATA ANALYSIS

The data collection effort for monolithic bipolar digital and linear devices has gathered approximately 20 billion hours of storage or non-operating field data with 270 device failures reported. In addition, 247 million plus hours of high temperature storage life data was collected with 711 device failures reported.

Ten data sources were used, two of which were reliability data banks, with the others representing specific programs. Field data included storage of missiles, warheads, satellite standby data and special parts testing programs.

4.1 General Data Analysis Discussion

The intent of the data analysis was to develop a stress level model which would be used to predict monolithic bipolar digital device failure rates in a non-operating environment. The MIL-HDBK-217B model used to predict operational failure rates for monolithic bipolar digital and linear SSI/MSI devices was used as a starting point for the non-operating model. The 217B model includes factors for learning, quality, temperature, application environment, and complexity as follows:

$$\lambda p = \Pi_L \Pi_Q \left[C_1 \Pi_T + C_2 \Pi_E\right]$$

where:

λ_p is the device failure rate.
Π_L is the learning factor.
Π_Q is the quality factor.
Π_T is the temperature acceleration factor.
Π_E is the application environment multiplier.
C_1, C_2 are the circuit complexity factors.

A first characterization of the storage or non-operating data identified a definite correlation between the device failure rate and the device quality and temperature. No significant difference was measured between the non-operating data for digital and linear device. Insufficient data was available to determine the effect of a learning factor or an application environment factor. The data on device complexity was analyzed but no significant differences were noted between the storage failure rate and the complexity of the device for SSI/MSI devices.

During the first characterization of the non-operating data, the failure experience indicated a sufficient difference between devices with aluminum metallization/aluminum wire systems and aluminum metallization/gold wire systems to require segregation of the data sets. This led to the segregation of data sets for other metallization/interconnection systems even though sufficient data was not available to completely characterize them.

The initial data characterization divided the data into several data sets with the prime category being metallization/interconnection systems, the first subcategory being quality level, and the second subcategory being ambient temperature. The data is shown in Tables 4-1 through 4-4 for devices with aluminum metallization/aluminum wire; aluminum metallization/gold wire; gold metallization/gold wire; and gold beam lead systems respectively.

Following this characterization, several other potential reliability factors were investigated. The results of the investigations indicated that no significant reliability difference was apparent in the data for storage duration, logic type, or package type. The data was insufficient to determine any factors for the die attach method or glassivation.

4.2 Real Time Storage Data and Variance

The real time storage data in Tables 4-1 through 4-4 is summarized in Table 4-5 with the calculated 90% one sided confidence limit on the failure rate. The less than symbol (<) indicates zero failure cases.

For devices with aluminum metal/aluminum wire, the Class

TABLE 4-1. DIGITAL/LINEAR NON-OPERATING DATA FOR DEVICES WITH ALUMINUM METALLIZATION/ALUMINUM WIRE

QUALITY LEVEL	AMBIENT TEMPERATURE	FUNCTION	STORAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS*
Class A	25-30°C	Digital	5,861.4	5	.85
		Linear	-	-	-
		Combined	5,861.4	5	.85
	125°C	Digital	.113	0	(<8850.)
		Linear	-	-	-
		Combined	.113	0	(<8850.)
	150°C	Digital	-	-	-
		Linear	.114	0	(<8772.)
		Combined	.114	0	(<8772.)
Class B	25-30°C	Digital	4,653.5	13	2.79
		Linear	2,018.8	9	4.46
		Combined	6,672.3	22	3.30
	125°C	Digital	.176	0	(<5682.)
		Linear	-	-	-
		Combined	.176	0	(<5682.)
	150°C	Digital	4.046	1	247.
		Linear	.139	0	(<7194.)
		Combined	4.185	1	239.
Class C	25-30°C	Digital	2,103.	8	3.8
		Linear	-	-	-
		Combined	2,103.	8	3.8
	125°C	Digital	.400	0	(<2500.)
		Linear	-	-	-
		Combined	.400	0	(<2500.)
	150°C	Digital	71.567	26	363.
		Linear	10.039	4	398.
		Combined	81.606	30	368.
	175°C	Digital	-	-	-
		Linear	6.289	8	1272.
		Combined	6.289	8	1272.
	180°C	Digital	.110	0	(<9091.)
		Linear	7.959	0	(<126.)
		Combined	8.069	0	(<124.)
	200°C	Digital	5.954	16	2687.
		Linear	3.034	1	330.
		Combined	8.988	17	1891
	250°C	Digital	3.100	23	7420.
		Linear	.338	3	8876.
		Combined	3.438	26	7564.
	300°C	Digital	3.656	59	16136.
		Linear	.292	3	10274.
		Combined	3.949	62	15701.
	350°C	Digital	2.152	148	68760.
		Linear	.069	4	58309.
		Combined	2.221	152	68438.

* Failures per billion hours.

TABLE 4-1. (Continued)

QUALITY LEVEL	AMBIENT TEMPERATURE	FUNCTION	STORAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
Class D	25-30°C	Digital	4.61	0	(<217.)
		Linear	-	-	-
		Combined	4.61	0	(<217.)
	100°C	Digital	-	-	-
		Linear	.01	0	(<100000.)
		Combined	.01	0	(<100000.)
	125°C	Digital	2.953	5	1693.
		Linear	-	-	-
		Combined	2.953	5	1693.
	150°C	Digital	53.702	46	857.
		Linear	15.496	19	1276.
		Combined	69.198	65	939.
	175°C	Digital	1.643	9	5479.
		Linear	-	-	-
		Combined	1.643	9	5479.
	180°C	Digital	.205	0	(<4878.)
		Linear	-	-	-
		Combined	.205	0	(<4878.)
	200°C	Digital	6.472	3	463.
		Linear	-	-	-
		Combined	6.472	3	463.
	300°C	Digital	.788	43	54358.
		Linear	.131	9	68702.
		Combined	.919	52	56574.
	350°C	Digital	-	-	-
		Linear	.041	29	710784.
		Combined	.041	29	710784.

TABLE 4-2. DIGITAL/LINEAR NON-OPERATING DATA
FOR DEVICES WITH ALUMINUM METALLIZATION/GOLD WIRE

QUALITY LEVEL	AMBIENT TEMPERATURE	FUNCTION	STORAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
Class A	250°C	Digital	.01	0	(< 100000.)
		Linear	-	-	-
		Combined	.01	0	(< 100000.)
	300°C	Digital	.01	0	(< 100000.)
		Linear	-	-	-
		Combined	.01	0	(< 100000.)
	350°C	Digital	.01	0	(< 100000.)
		Linear	-	-	-
		Combined	.01	0	(< 100000.)
Class B	25-30°C	Digital	2604.11	77	30.
		Linear	114.0	6	53.
		Combined	2718.11	83	31.
Class C	150°C	Digital	15.848	50	3155.
		Linear	2.88	6	2083.
		Combined	18.728	56	2990.
	175°C	Digital	.282	0	(< 3546.)
		Linear	-	-	-
		Combined	.282	0	(< 3546.)
	200°C	Digital	.758	9	11873.
		Linear	-	-	-
		Combined	.758	9	11873.
	250°C	Digital	.315	13	41270.
		Linear	-	-	-
		Combined	.315	13	41270.
Class D	25-30°C	Digital	.268	0	(< 3731.)
		Linear	-	-	-
		Combined	.268	0	(< 3731.)
	125°C	Digital	.307	0	(< 3257.)
		Linear	-	-	-
		Combined	.307	0	(< 3257.)
	150°C	Digital	20.015	31	1549.
		Linear	.896	4	4463.
		Combined	20.911	35	1674.
	180°C	Digital	.086	7	81112.
		Linear	-	-	-
		Combined	.086	7	81112.
	200°C	Digital	.119	40	336417.
		Linear	-	-	-
		Combined	.119	40	336417.
	250°C	Digital	.068	99	1462000.
		Linear	-	-	-
		Combined	.068	99	1462000.

TABLE 4-3. DIGITAL NON-OPERATING DATA FOR DEVICES WITH GOLD METALLIZATION/GOLD WIRE

QUALITY LEVEL	AMBIENT TEMPERATURE	STORAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
Class B	25-30°C	.354	0	(<2825.)
Class C	25-30°C	8.689	0	(<115.)
Class D	25-30°C	8.689	0	(<115.)

TABLE 4-4. DIGITAL NON-OPERATING DATA FOR GOLD BEAM SEALED JUNCTION DEVICES

QUALITY LEVEL	AMBIENT TEMPERATURE	STORAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
Class B	150°C	.045	0	(<22200.)
Class D	150°C	2.41	0	(<415.)
	200°C	2.13	1	469.
	300°C	.062	0	(<16200.)

TABLE 4-5. FIELD FAILURE RATE DATA

TYPE	QUALITY LEVEL	FAILURE RATE IN FITS BEST ESTIMATE	90% ONE-SIDED LIMIT
Aluminum Metal/ Aluminum Wire	Class A	.85	1.6
	Class B	3.3	4.4
	Class C	3.8	6.2
	Class D	(<217.)	501.
Aluminum Metal/ Gold Wire	Class A	-	
	Class B	31.	35.4
	Class C	-	
	Class D	(<3731.)	8617.
Gold Metal/ Gold Wire	Class A	-	
	Class B	(<2825.)	6500.
	Class C	(<115.)	266.
	Class D	(<115.)	266.

TABLE 4-6. SPECIAL STORAGE ENVIRONMENT DATA*

QUALITY LEVEL	AMBIENT TEMPERATURE	FUNCTION	STORAGE HRS. X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
B-A	22°C	Digital	1272.6	97	76.2
B-A	22°C	Linear	291.4	21	72.1

*Stored in Nitrogen Atmosphere.

A failure rate is 0.85 fits (failures per billion hours). The Class B devices show a failure rate approximately 3.5 times the Class A device and Class C devices approximately 4.5 times the Class A device. The only device quality level having sufficient failures to show a range were the Class B devices. For data sets indicating failures, the data ranged from 1.3 to 14.5 fits for digital devices and from 2.7 to 8.5 fits for linear devices.

One group of data was separated due to its special storage environment and is shown in Table 4-6. See the discussion of data source H in Section 4.5.

For devices with aluminum metal/gold wire, only Class B device data was sufficient for prediction at 31.0 fits. The failure rate for Class B devices ranged from 18.2 to 65.3 fits in data sets which indicated failures. These devices are older devices and may not be representative of current Al/Au devices. However, data from recent programs on low complexity hybrid devices with Al/Au interfaces at the interconnections show continued problems with wire bonds. One program included 10,580 devices (approximately quality Class A) stored in an environmentally controlled nitrogen atmosphere for 1.4 years with 2 wire bond failures. The other was a missile program with 36,138 devices (Class B) stored in the field for 1.5 years with 19 wire bond failures. These programs show failure rates of 14.8 fits and 40.0 fits respectively.

Insufficient real time storage data is available on gold metal, gold wire devices to make a detailed estimate. Pooling all the quality level data results in a failure rate of less than 56.0 fits.

4.3 Principle Failure Mechanisms

Little detailed data on failure mechanisms was available for the 132 field failures reported. Those reported included: 4 oxide defects, 5 wire bond defects due to Kirkendall voiding and intermetallics, and 3 cracked dies. Seventy seven failures were categorized as catastrophic, 15 as contamination and one as metal corrosion with no further details.

In addition, 31 failures were noted as a vendor related problem with interconnection wires contacting the chip periphery. The data set with these 31 failures was excluded from the analysis since they did not represent the general class of these devices.

User surveys indicated the following as principle failure mechanisms: wire bonding, metallization corrosion, intermetallic compound formations, oxide defects, and shorts from loose conductive particles in the package.

Failure mechanisms for 28 of the 372 high temperature storage life test failures of aluminum metallization/aluminum wire devices were reported. Principle problems were oxide defects and wire bond failures. Other mechanisms reported included diffusion defects, surface inversion, aluminum-gold post bond failures, die bond failures and lead failures. The percentage of each of these is presented in Table 4-7.

Both the oxide defects and wire bond failures are primarily a result of process defects. Strict control of surfaces, masks, etc., for cleanliness and control of etch times, bonding times, process temperatures, pressures, etc., prevent most of these defects from occurring. However, the screens must be capable of weeding out those defects which slip past the controls. The primary screen or quality conformance testing used to detect oxide defects include: visual inspection, operating D. C. and temperature, operating A. C. and temperature, high temperature reverse bias, power cycling, and elevated temperature storage. For aluminum wire bond defects, the tests include: Temperature Shock/Cycle, operating D. C. and temperature, elevated temperature storage, centrifuge, mechanical shock, and bond pull tests. Each of these screens must be used with care, however, to prevent fatigue and degradation of good devices.

Failure mechanisms for aluminum metallization/gold wire devices are also presented in Table 4-7. In this case, failure

mechanisms for 155 of the 243 high temperature storage life test failures were reported. The wire bond problem accounting for almost 80% of these failures.

The gold wire to aluminum bond suffers from interface problems between dissimilar metals. The time/temperature effects of intermetallic compound formation and voiding around the bond as a result of the Kirkendall effect require strict design and process control for the device. Studies have indicated that these effects are reduced significantly when the gold wire thickness at the heel is greater than six times the metallization thickness. The purity of the gold is also reported as an important factor in gold wire-aluminum bonds.

Screening and quality conformance tests used to detect and weed out weak gold-aluminum bonds include: temperature shock/cycle, elevated storage temperature, operating D. C. and temperature, mechanical shock, centrifuge, and bond pull tests. Temperature shocks and thermal cycling at temperatures above 200°C have been reported to degrade good bonds.

The field data is insufficient to quantify the ratio of failure mechanism occurrences. However, the user survey and high temperature storage life test data indicates that the ratio of occurrence is not significantely different than those experienced in the operating environment. No mechanisms peculiar to storage have been identified.

4.4 Failure Rate Factor Development

The non-operating data was classified where possible according to the device classifications identified in Section 3. Data primarily was available on quality level, storage temperature, complexity, test or storage duration, logic type, die attach method and glassivation. The following sections describe the data for each of the 217B factors and these additional factors and correlate it with the device failure rate.

4.4.1 Learning Factor (π_L)

The learning factor, π_L, used in MIL-HDBK-217B, adjusts the failure rate where: 1) a new device is in initial production; 2) where major changes in design or process have occurred;

and 3) where there has been an extended interruption or a change in line personnel. For each of these situations, the 217B model uses a π_L factor of 10 for up to 6 months of production. Otherwise the π_L factor is 1.

Of the non-operating data collected, either an established production line was identified or no identification of the production stage was given. Therefore, a π_L factor of 1 was assumed on all data collected.

4.4.2 Quality Class

Four quality classes or levels are defined in this data. Classes A, B and C refer to MIL-STD-883 quality levels and Class D is used for the manufacturer's commercial quality level. The classes are described in Section 3.3.

The major differences in Classes A, B and C are in the screening procedures and quality conformance testing.

Screens required for Class B which are not required for Class C include precap visual, burn-in tests; static tests at minimum and maximum operating temperatures, and dynamic tests. Screens required for Class A which are not required for Class B include: thermal shock, mechanical shock, reverse bias burn-in (when specified for Class A), and radiographic examinations. Also the precap visual, constant acceleration and burn-in tests are more severe for Class A than Class B.

The types of quality conformance testing for the three quality classes are practically identical except that operating life tests and steady state reverse bias tests required for Class A devices are not required for Class B and C devices. The primary difference in the quality conformance testing is the number of defectives allowed in each test. The most defectives are allowed in Class C while the least defectives are allowed in Class A.

Class A devices also require a certified production line.

While the majority of the data collected identified devices according to a quality level (A, B, C, or D), some of the data included detailed procurement specifications. Comparison of the specifications to MIL-STD-883 indicated that these particular devices were equivalent to Class B devices

TABLE 4-7. PRINCIPLE FAILURE MECHANISMS

Aluminum Metallization, Aluminum Wire, Gold Post

Oxide Defects (31%)
Wire Bond (19%)
Diffusion Defects (16%)
Surface Inversion (13%)
Al-Au Post Bond (12&)
Die Bond (3%)
Lead Failures (6%)

Aluminum Metallization, Gold Wire, Gold Post

Wire Bond (76%)
Resistive Output (16%)
Oxide Defects (4%)
Die Bond (2%)
Wire Shore (2%)
Cracked Die (1%)

with extra testing. In the data analysis, these devices were included as Class B because the extra testing did not bring them up totally to Class A requirements. Failure experience on these devices was insifficient to measure the effect of the extra testing.

4.4.2.1 Aluminum Metal/Aluminum Wire System Quality Factors (Π_Q)

At ambient temperatures of 25 to 30° centigrade, Class A devices exhibited a failure rate of 0.00085 failures per million hours, Class B devices at a rate of 0.0033 failures per million hours, and Class C devices a rate of 0.0038 failures per million hours. Using Class A as the base, the Class A Π_Q factor was defined as 1. The Class B Π_Q factor was then calculated as approximately 3.5, and the Class C Π_Q factor as 4.5. Insufficient field data was available for Class D devices, however, comparisons of Class C and D devices were made for the 150°C and 300°C high temperature storage tests. These indicated a factor of approximately 2.5 between Class C and Class D. Using Class A as base, the Class D Π_Q factor equivalent was determined to be approximately 11.25.

4.4.2.2 Aluminum Metal/Gold Wire System Quality Factors (Π_Q)

Data on aluminum metal/gold wire failures for each quality level contained too few failures to make a direct calculation of all these factors. For the difference between Class C and Class D, the high temperature storage tests at 200°C and 200°C and 250°C were compared. These indicated a factor of approximately 30 between Classes C and D. Initial estimates were made on Class B and Class C Π_Q factors consistent with that of the all-aluminum system. Setting the Class A Π_Q factor equal to 1, the Class B Π_Q factor equal to 3.5, and the Class C Π_Q factor equal to 4.5, the Class D Π_Q factor was calculated to be approximately 135.

4.4.2.3 Gold and Gold Beam Lead System Quality Factors (Π_Q)

Data collected on gold and gold beam lead metallization/interconnection systems contained only one reported failure. No attempt was made to estimate quality factors for these devices.

4.4.3 Temperature Effects

Analysis of the collected data indicated that the Arrhenius model commonly used for all semiconductors is appropriate to use with the storage data. This model is the so called "law of thermal degradation" which says that the natural log of the basic failure rate is a function of the negative reciprocal of the absolute junction temperature. The form of the temperature effect used in MIL-HDBK-217B is:

$$\Pi_L \Pi_Q C_1 \Pi_T$$

where: Π_L is the learning factor.
Π_Q is the quality factor.
C_1 is the complexity factor.

$$\Pi_T = 0.1 \exp\left[-a\left(\frac{1}{T + 273} - \frac{1}{298}\right)\right]$$

a is a constant depending on the device type.
T is the junction temperature in degrees centigrade.

The failure rate model of MIL-HDBK-217B assumes the effects of temperature and application environment are additive and independent. An analysis of the model indicates that at 25°C the application environment (mechanical stress) effects are the dominant element of the failure rate and the temperature effect gradually becomes the dominant element at temperatures of 75°C and higher depending on the device.

The storage data analyzed contained data at 25-30°C in the field and high temperature storage life data from 125°C to 350°C. Based on the 217B model analysis, the data points at 25-30°C were omitted in the Π_T calculation. Following calculation of the Arrhenius model factors, it was verified that the failure rates at 25-30°C were higher than those projected from the Arrhenius fit to the high temperature data. This indicated that the field failures are a function of the temperature plus the mechanical stresses experienced in the application environment.

4.4.3.1 Aluminum Metal/Aluminum Wire System Temperature Factor (Π_T)

Figure 4-1 presents the Arrhenius model fit to the high temperature storage life test data for devices with aluminum metal/aluminum wire systems. All of the high temperature storage data was normalized to Class A via the Π_Q factors and used to calculate the model. Calculating the coefficient of correlation between the Class C data points and the Arrhenius fit gave a coefficient of 0.98. For the Class D data points, a coefficient of correlation of 0.53 was calculated. The high temperature data on Class A and B devices was insufficient to determine a correlation to the Arrhenius model.

The temperature factor, Π_T, for devices with aluminum metal/aluminum wire systems is defined as follows for this report:

$$\Pi_T = 0.1 \exp\left[-6608\left(\frac{1}{T+273} - \frac{1}{298}\right)\right]$$

with a complexity factor, C_1, of 0.00135.

Figure 4-1 presents the Arrhenius model for Class C & Class D based on the Π_T and the Π_Q factors calculated in Section 4.4.2.

4.4.3.2 Aluminum Metal/Gold Wire System Temperature Factor (Π_T)

Figure 4-2 presents the Arrhenius model fit to the high temperature storage life test data for devices with aluminum metal/gold wire systems. In this case, more Class D data was available than Class C. Normalizing the Class D data to Class C based on the quality factor, Π_Q, an Arrhenius fit was made to both Class C and Class D data. The coefficient of correlation for the Class C data points to the Arrhenius fit was calculated as 0.81 and for the Class D data points as 0.96. High temperature data on Class A and Class B devices was insufficient to determine a correlation to the Arrhenius model.

The temperature factor, Π_T, for devices with aluminum metal/gold wire systems is defined as follows for this report:

$$\Pi_T = 0.1 \exp\left[-10502\left(\frac{1}{T+273} - \frac{1}{298}\right)\right]$$

with a complexity factor, C_1, of 0.000034

Figure 4-2 presents the Arrhenius model for Class C and Class D based on the Π_Q factors calculated in Section 4.4.2.

4.4.3.3 Gold and Gold Beam Lead Systems Temperature Factors (Π_T)

The data collected on gold and gold beam lead systems does not have enough failure experience to estimate a temperature factor.

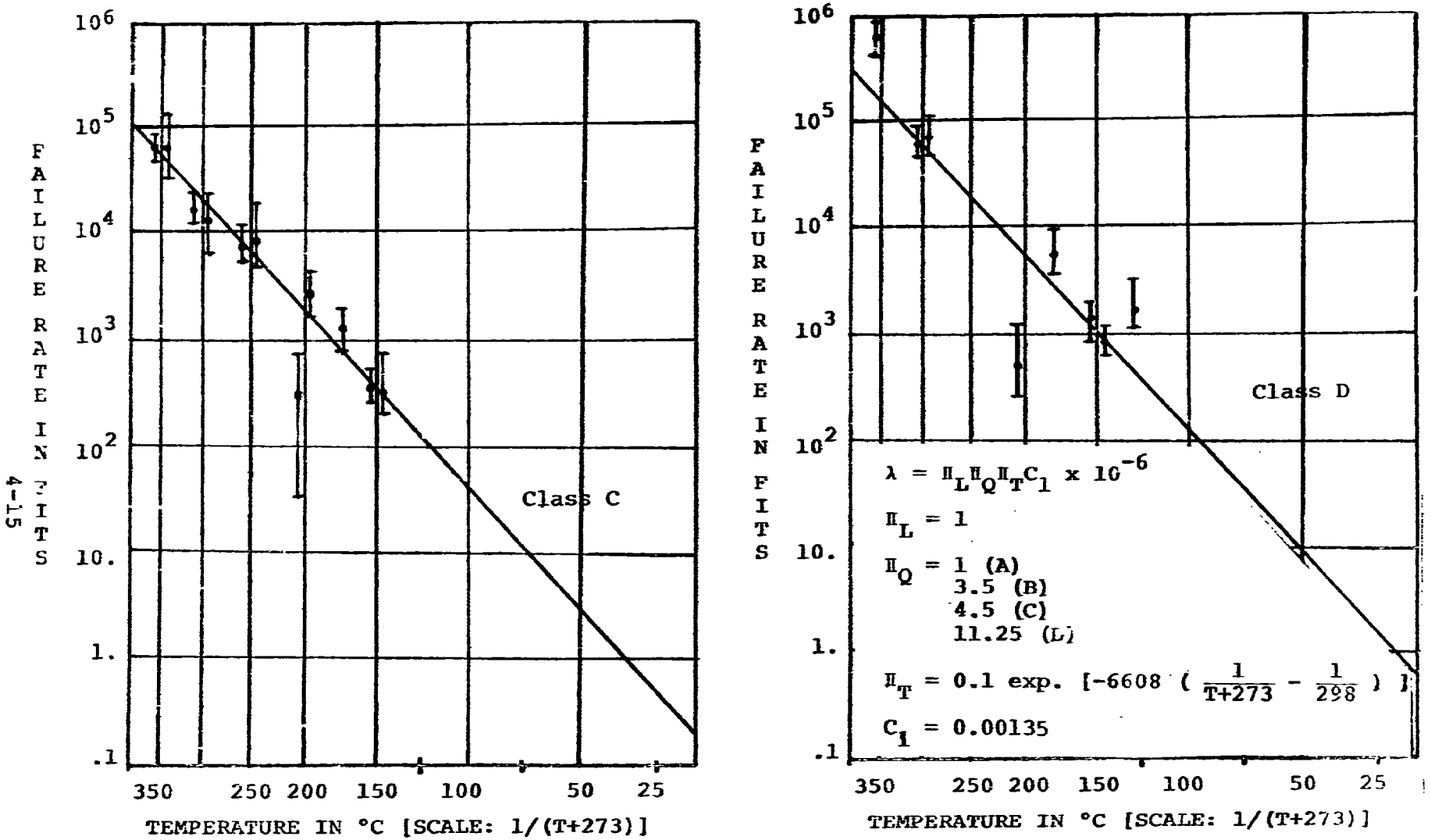


FIGURE 4-1. ARRHENIUS FIT FOR ALUMINUM METAL/ALUMINUM WIRE SYSTEM

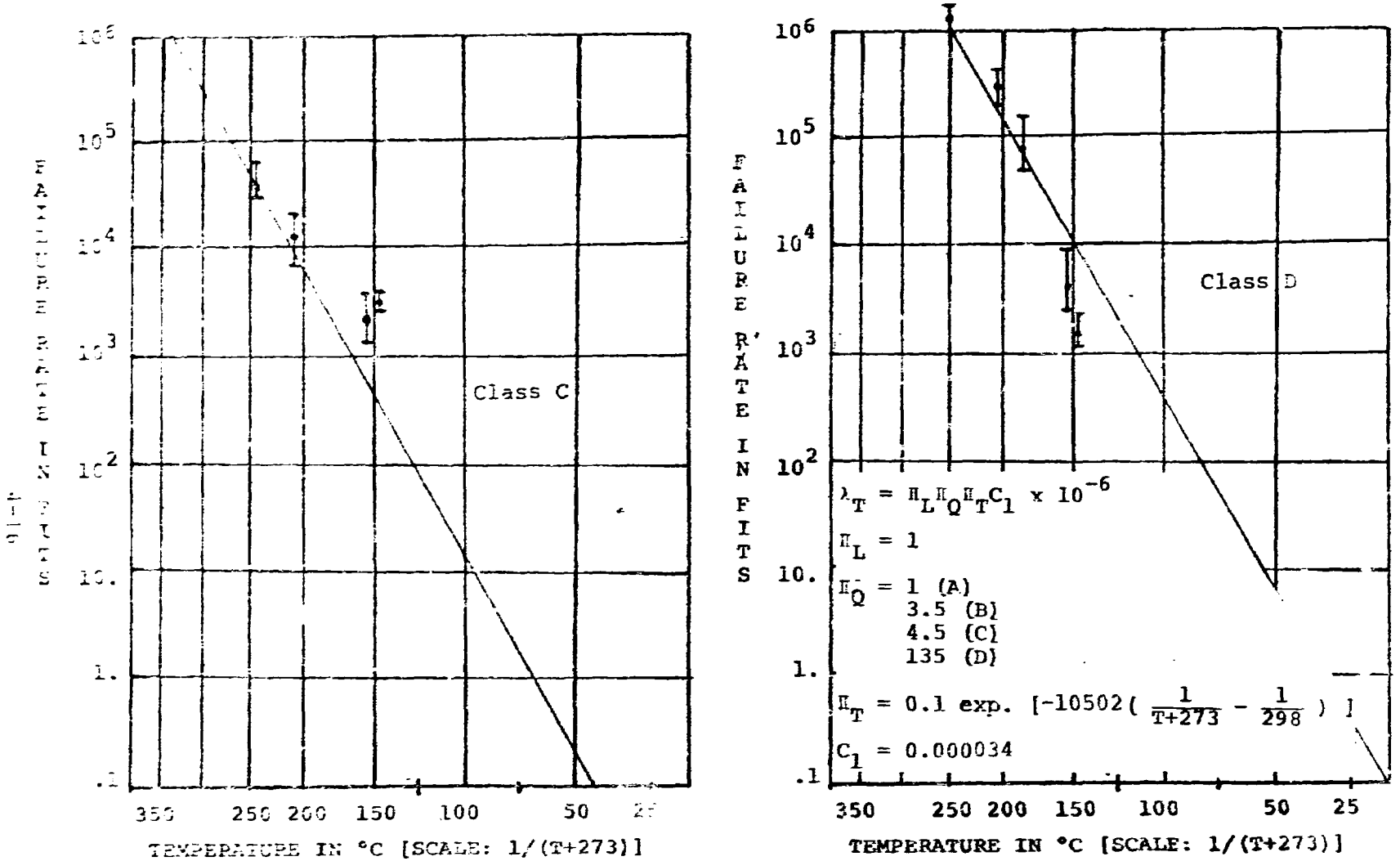


FIGURE 4-2. ARRHENIUS FIT FOR ALUMINUM METAL/GOLD WIRE SYSTEM

4.4.4 Application Environment Factor (Π_E)

The non-operating data collected was primarily fixed ground storage with little detail on the effects of transportation, handling, etc. One set of data identified the transportation environments but no failures were reported in that data set.

An application environment factor, Π_E, of 1 was used in the data analysis, consistent with the MIL-HDBK-217B ground, fixed environment factor.

4.4.5 Temperature Complexity Factor (C_1)

The MIL-HDBK-217B model defines complexity factors in an operational environment for both temperature accelerated failures and environment accelerated failures. These factors indicated a failure rate of 2 to 6 times for a high complexity device (up to 100 gates) versus a low complexity device. The factors depend on the device type, environment and temperature.

A like correlation was investigated in the non-operating data. The data was segregated into three complexity levels with level 1 representing devices with up to 5 gates/20 transistors (SSI); level 2 from 6 to 11 gates/21 to 44 transistors (SSI); and level 3 from 12 to 20 gates/45 to 80 transistors with a few data points at 25 and 60 gates (MSI).

4.4.5.1 Aluminum Metal/Aluminum Wire System Complexity Correlation

Figure 4-3 presents a plot of the data points of three device complexity levels with an aluminum metal/aluminum wire system. These data points represent Class C devices and the line plotted in Figure 4-3 is the Arrhenius fit for the Class C data. As indicated in the figure, the level 3 data points tend to show a lower failure rate rather than the expected higher failure rate. The data used for this plot is presented in Table 4-8.

Calculating a coefficient of correlation between the data points and the Arrhenius model gave coefficients of 0.97 for level 1; 0.99 for level 2 and 0.76 for level 3 devices. From this analysis, the complexity factor, C_1, is determined to be constant and equal to 0.00135 as calculated in Section 4.4.3.1.

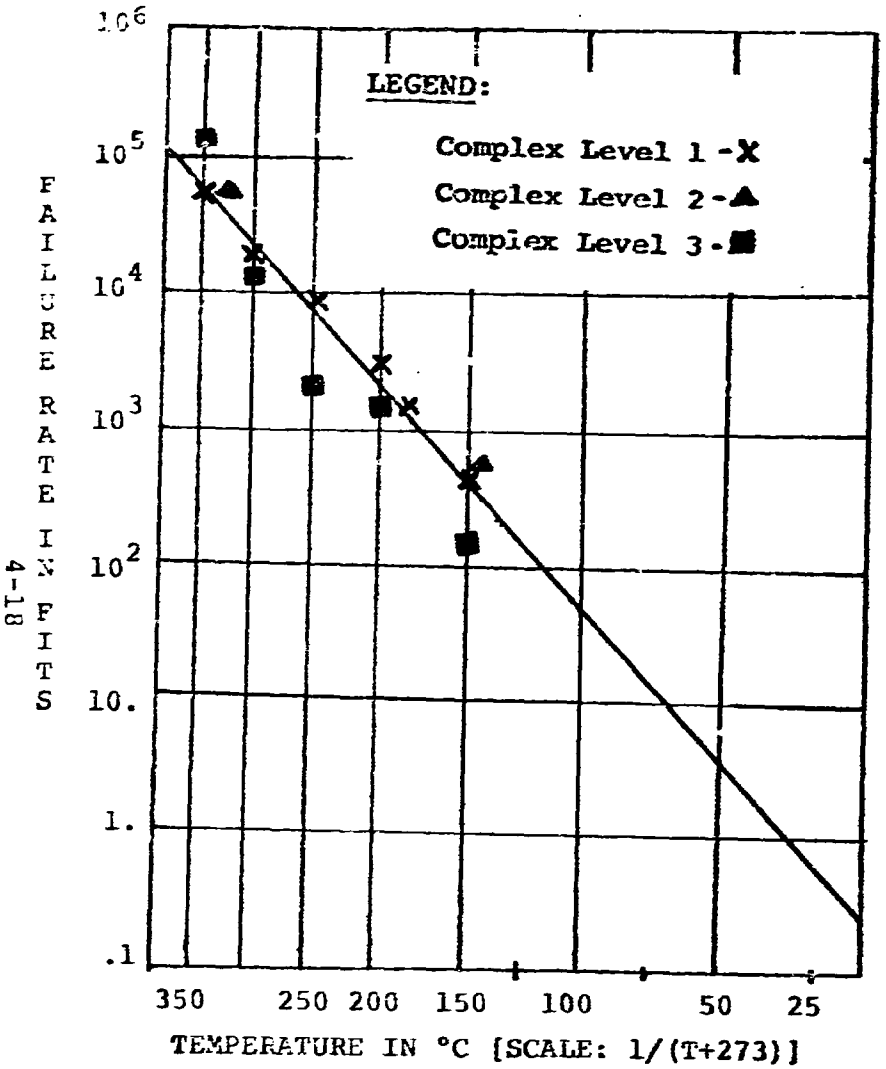


FIGURE 4-3. COMPLEXITY CORRELATION FOR ALUMINUM METAL/ALUMINUM WIRE SYSTEM (CLASS C)

TABLE 4-8. ALUMINUM METAL/ALUMINUM WIRE COMPLEXITY DATA (CLASS C)

TEMPERATURE	COMPLEXITY LEVEL	STORAGE HRS. X 10^6	NO. FAILED	FAIL. RATE IN FITS
125°C	2	.4	0	(<2500.)
150°C	1	39.876	16	401.
	2	18.859	11	583.
	3	22.542	3	133.
175°C	1	6.289	8	1272.
180°C	1	.149	0	(<6711.)
	2	7.92	0	(<126.)
200°C	1	5.579	16	2868.
	2	2.796	0	(<358.)
	3	.598	1	1672.
250°C	1	2.701	25	9255.
	2	.245	0	(<4080.)
	3	.491	1	2036.
300°C	1	2.944	57	19362.
	2	.626	0	(<1597.)
	3	.379	5	13210.
350°C	1	1.665	92	55272.
	2	.247	15	60630.
	3	.309	45	145584.

4.4.5.2 Aluminum Metal/Gold Wire System Complexity Correlation

Figure 4-4 presents a plot of the data points of three device complexity levels with an aluminum metal/gold wire system. These data points represent Class C devices and the line plotted in Figure 4-4 is the Arrhenius fit for the Class C data.

In the figure, the data points at 150°C and 250°C indicate a possible correlation between failure rate and complexity. However, this data is insufficient to make any positive correlation. A comparison of Class D data was also made which also indicated a possible correlation. The calculated failure rates for various device classes and temperatures yielded factors of 1.8 to 3.5 between complexity level 1 and level 3 devices. The data used for this comparison is presented in Table 4-9.

For this report, it was determined to use a constant complexity factor for C_1 which was calculated as 0.000034 Section 4.4.3.2.

4.4.6 Time Dependency

The storage or non-operating models analyzed assume a constant failure rate over the device storage period and the predicted reliability distribution is exponential. Using the high temperature storage life test data, this assumption was investigated. Figures 4-5 and 4-6 present plots of non-operating failure rates calculated for different test durations for aluminum metal/aluminum wire and aluminum metal/gold wire systems respectively. Tables 4-10 and 4-11 list the data used for these plots. The high temperature storage data included durations of 1000 hours to 2-1/3 years. No significant trend is apparent from the data to indicate that the failure rate is not constant.

4.4.7 Logic Type and Function Correlation

The data collected was primarily on three logic types: Transistor-Transistor Logic (TTL), Diode-Transistor Logic (DTL) and Resistor-Transistor Logic (RTL). An investigation of the high temperature storage life test data was made to

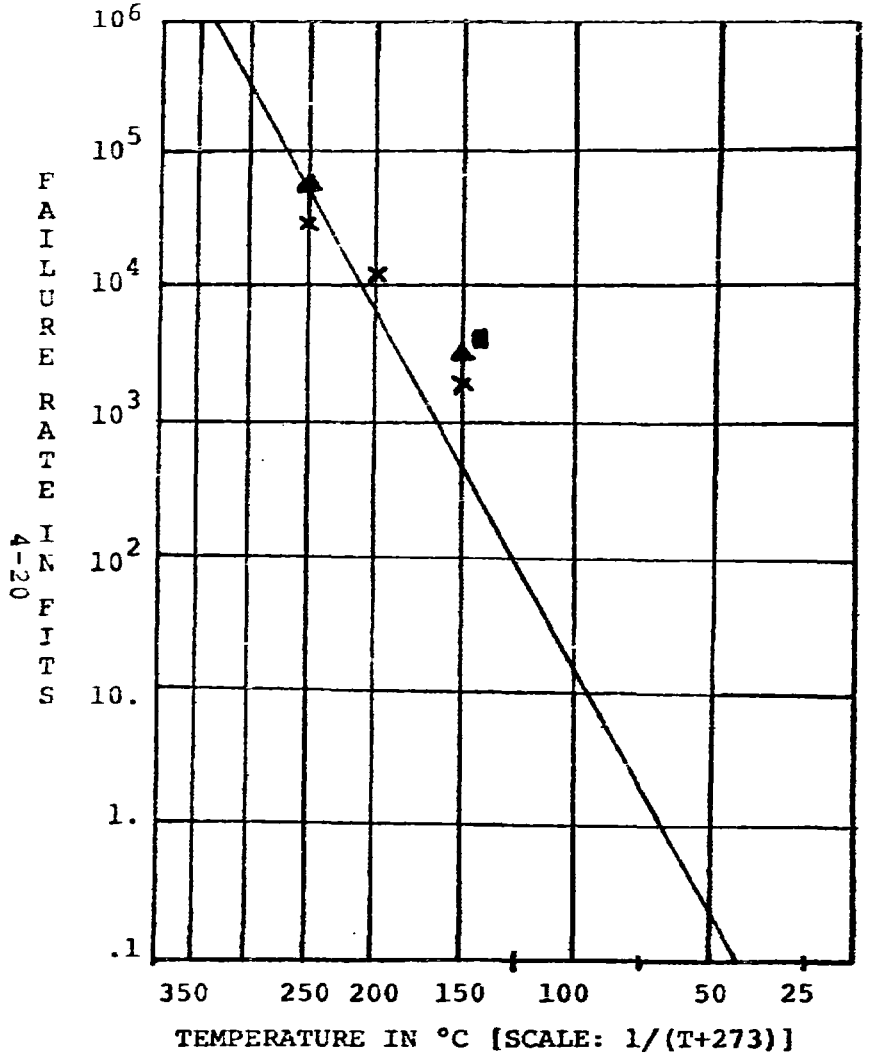


FIGURE 4-4. COMPLEXITY CORRELATION FOR ALUMINUM METAL/GOLD WIRE SYSTEM (CLASS C)

TABLE 4-9. ALUMINUM METAL/GOLD WIRE COMPLEXITY DATA

CLASS	TEMP	COMPLEXITY LEVEL	STORAGE HRS. X 10^6	NO. FAILED	FAIL. RATE IN FITS
C	150°C	1	4.532	9	1986.
		2	13.18	42	3187.
		3	1.016	5	4921.
	175°C	1	.282	0	(<3546.)
	200°C	1	.758	9	11873.
	250°C	1	.22	7	31818.
		2	.095	6	63158.
D	125°C	1	.145	0	(<6896.)
		2	.125	0	(<8000.)
		3	.037	0	(<27027.)
	150°C	1	3.514	8	2277.
		2	16.63	23	1383.
		3	.767	4	5215.
	180°C	1	.029	1	34602.
		3	.057	6	104530.
	200°C	3	.119	40	336417.
	250°C	1	.031	31	1003000.
		3	.037	68	1847000.

LEGEND: Complex Level 1-X
Complex Level 2-▲
Complex Level 3-■

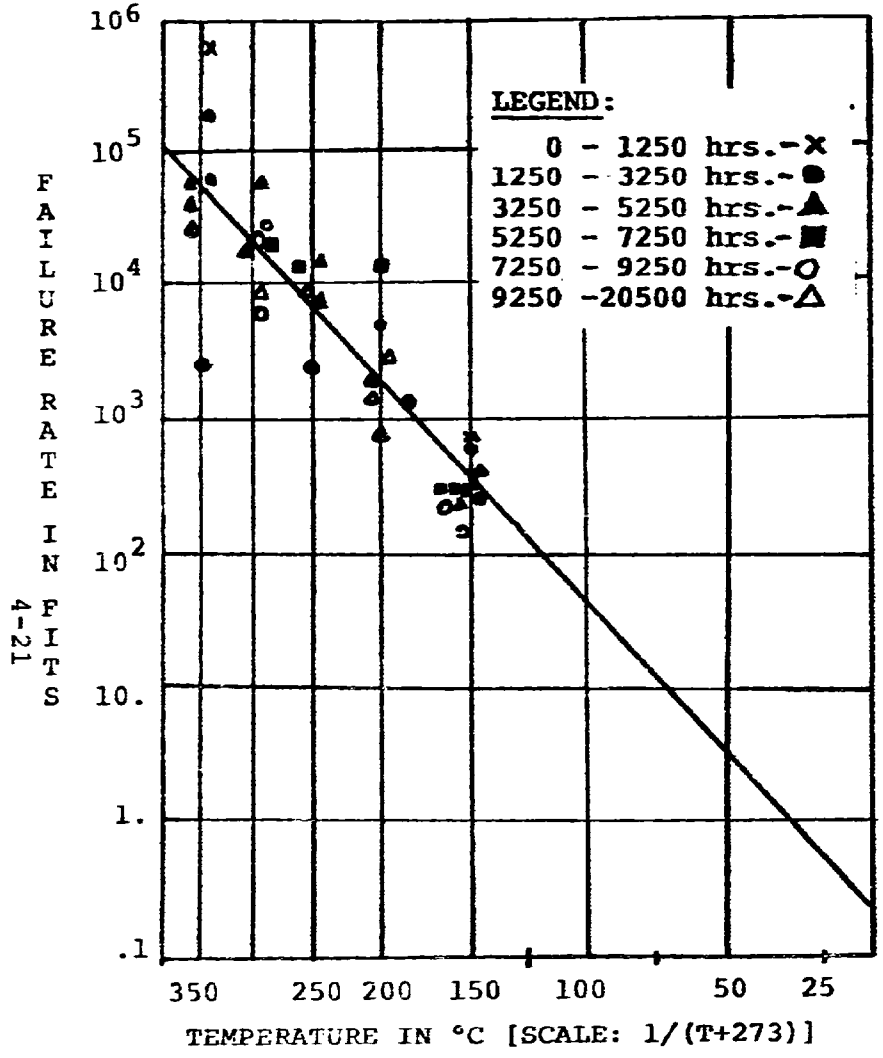


FIGURE 4-5. TEST DURATION CORRELATION FOR ALUMINUM METAL/ALUMINUM WIRE SYSTEM (CLASS C)

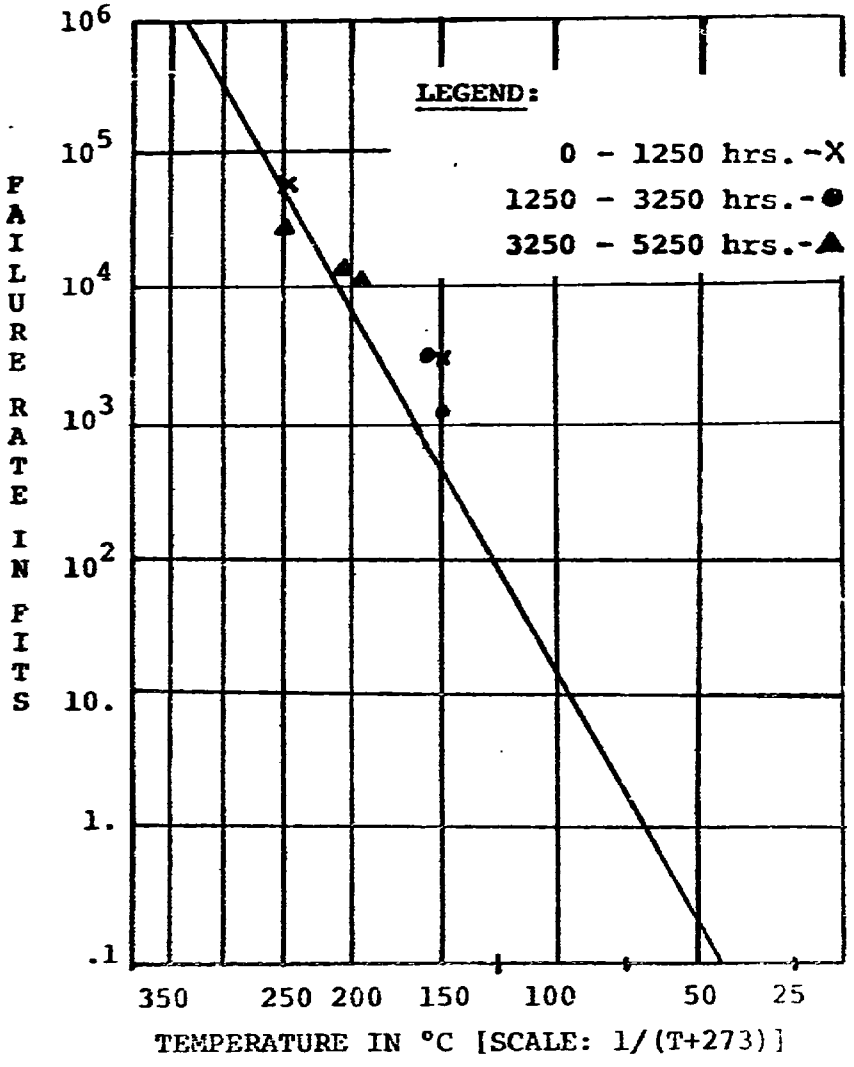


FIGURE 4-6. TEST DURATION CORRELATION FOR ALUMINUM METAL GOLD WIRE SYSTEM (CLASS C)

TABLE 4-10. ALUMINUM METAL/ALUMINUM WIRE TEST DURATION FAILURE DATA (CLASS C)

TEMP	TEST DURATION	STORAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
125°c	1000	.4	0	(<2500.)
150°C	1000	7.919	7	884.
	1500	3.675	1	272.
	2000	1.577	0	(<634.)
	2500	6.23	2	321.
	3000	5.67	4	705.
	3500	28.125	7	249.
	4000	9.31	4	430.
	5500	6.13	2	326.
	7000	2.86	1	350.
	7500	3.86	1	259.
	8000	6.26	1	160.
175°C	1000	.449	0	(<2227.)
	1500	5.84	8	1370.
180°C	1000	.149	0	(<6711.)
	3000	.03	0	(<33333.)
	12000	7.89	0	(<127.)
200°C	1000	.015	0	(<66225.)
	2000	2.7	0	(<370.)
	3000	.19	1	5271.
	4500	1.08	1	926.
	5000	.484	1	2066.
	6500	.555	8	14414.
	9000	1.31	0	(<763.)
	10000	.504	0	(<1984.)
	13000	1.54	5	3247.
	20500	.61	1	1639.
250°C	1000	.03	0	(<33000.)
	3000	.447	1	2239.
	4000	.338	3	8876.
	4500	.067	1	15037.
	5000	.15	0	(<6667.)
	5500	.435	0	(<2299.)
	6000	1.149	16	13952.
	7000	.072	0	(<13889.)
	10000	.2	0	(<5000.)
	11000	.55	5	9091.
300°C	1000	.015	0	(<66200.)
	2000	.25	6	23981.
	4000	.131	9	68702.
	4500	.086	0	(<11574.)
	5000	.097	2	20682.
	7000	1.386	31	22366.
	8000	.28	8	28571.
	8500	.69	4	5800.
	12000	.852	8	9390.
350°C	1000	.086	58	670000.
	2000	.129	28	217600.
	2500	.644	43	66700.
	3000	.403	1	2481.
	3500	.49	29	59180.
	4500	.04	1	25250.
	5000	.402	17	42290.

TABLE 4-11. ALUMINUM METAL/GOLD WIRE
TEST DURATION FAILURE DATA (CLASS C)

TEMPERATURE	TEST DURATION (HRS.)	STORAGE HOURS $\times 10^6$	NUMBER FAILED	FAILURE RATE IN FITS
150°C	1000	17.626	54	3064.
	1500	.816	1	1225.
	2000	.286	1	3496.
175°C	3000	.282	0	(3546.)
200°C	4000	.188	2	10638.
	4500	.57	7	12281.
250°C	1000	.095	6	63158.
	5000	.22	7	31818.

determine if the logic type or function had any effect on the failure rate. Figures 4-7 and 4-8 present plots of non-operating failure rates calculated for different logic types and functions for aluminum metal/aluminum wire and aluminum metal/gold wire systems respectively. Tables 4-12 and 4-13 list the data used for these plots.

For aluminum metal/aluminum wire systems, the DTL devices tended to have a lower failure rate than the RTL, TTL and linear devices. However, the with the scatter, no definite correlation was made.

For the aluminum metal/gold wire systems, no discernable difference was apparent between TTL, DTL and linear devices.

4.4.8 Package Type Correlation

In report MCR-72-169, "Long-Life Assurance Study for Manned Spacecraft Long-Life Hardware" dated December 1972, the TO-type can and the flat pack were the only packages recommended for high reliability, long life use. The dual-in-line package was not recommended due to 1) excess strain in the glass seal area from the heavy lead materiel, 2) excess torque on the seal during insertion or flexing of the circuit board and 3) thermal conduction through the leads since the body is not in contact with the surface.

The non-operating data was investigated to determine if any difference in reliability could be determined for the various package types. Figures 4-9 and 4-10 present plots of non-operating failure rates calculated for different package types for aluminum metal/aluminum wire and aluminum metal/gold wire systems respectively. Tables 4-14 and 4-15 list the data used for these plots.

The abbreviations in the figures and tables are defined as: CAN (TO type metal can); CDIP (Ceramic Dual in-line); EDIP (Epoxy dual in-line); CMDIP (Ceramic metal dual in-line); PDIP (phenolic dual in-line); SDIP (silicone dual in-line); FPCM (flat pack ceramic); FPM (Flat pack metal); and FPG (flat pack glass).

The plots indicate no significant difference in the failure rates for the various package types. Both plots indicate a higher failure rate for dual-in-line packages at 150°C, however, this point in Figure 4-9 is based on only 52,000 hours with one failure and in Figure 4-10 on only 326,000 hours with 2 failures. Class D data on package types is also included in Tables 4-13 and 4-14 since more data is available on these type packages. The most data on dual in-line packages is Class D at 150°C and 300°C for the all-aluminum system and Class D at 150°C for the aluminum/gold system. In one case, the dual in-line failure rate is higher than the flat pack or can, in another case lower and in the third case less than the can but higher than the flat pack. With this scatter, no difference in the failure rate of dual in-line packages can be determined.

Data on phenolic and epoxy dual in-line packages are also presented in Tables 4-13 and 4-14. This limited data on plastic packages seems to be in the same ball park as the hermetic packages except for the data for Class D all-aluminum system at 150°C. Here the phenolic dual in-line package shows a higher failure rate, although the sample of 3 failures is small. At the same temperature, the epoxy dual in-line package shows no failures after one million hours.

From this investigation, no significant difference can be identified at this time in the failure rates for various type packages.

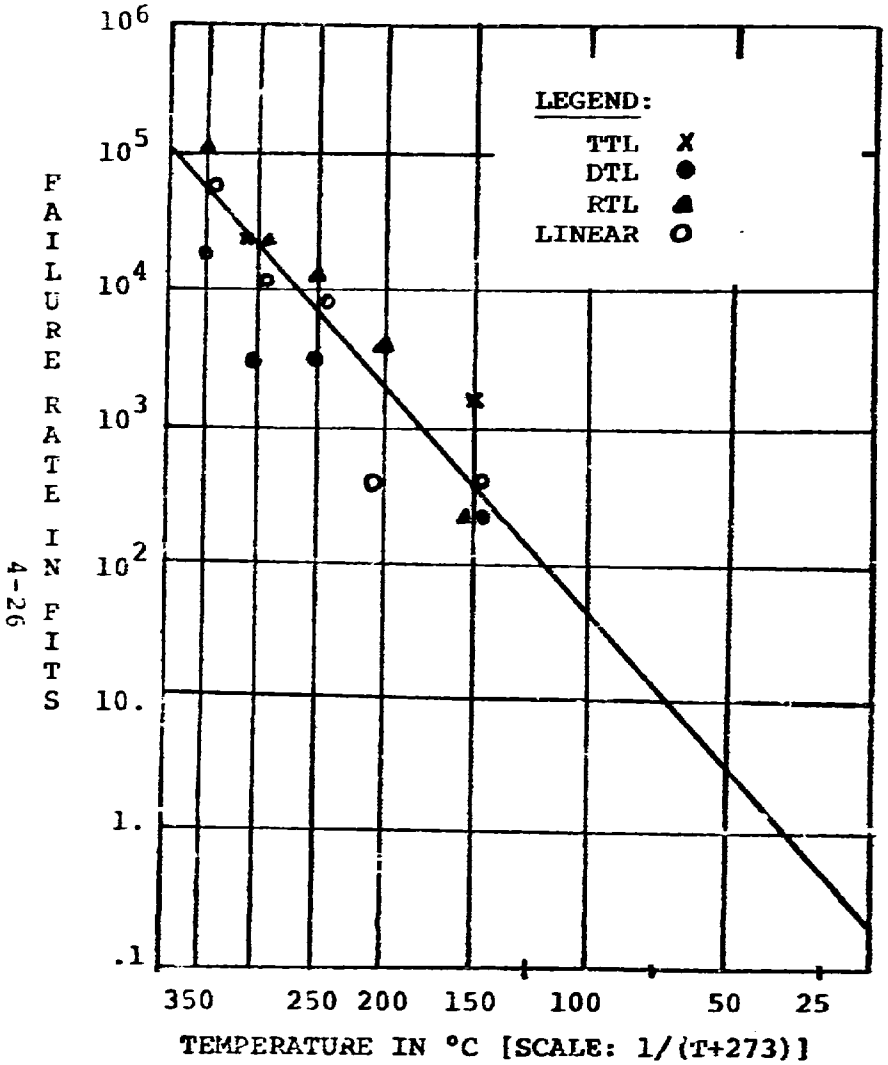


FIGURE 4-7. FUNCTION AND LOGIC TYPE CORRELATION FOR ALUMINUM METAL/ALUMINUM WIRE SYSTEM (CLASS C)

TABLE 4-12. ALUMINUM METAL/ALUMINUM WIRE FUNCTION AND LOGIC TYPE DATA (CLASS C)

TEMP	FUNCTION OR LOGIC TYPE	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
125°C	TTL	.4	0	(<2500.)
150°C	RTL	45.154	11	244.
	TTL	5.562	10	1798.
	DTL	22.202	5	225.
	LIN.	10.039	4	398.
180°C	TTL	.11	0	(<9091.)
200°C	RTL	3.894	16	4109.
	TTL	.15	0	(<6667.)
	DTL	1.91	0	(<524.)
	LIN.	3.034	1	330.
250°C	RTL	1.357	17	12530.
	TTL	.178	0	(<5624.)
	DTL	1.565	5	3195.
	LIN.	.338	3	8876.
300°C	RTL	2.017	49	24290.
	TTL	.237	6	25350.
	DTL	1.402	4	2852.
	LIN.	.292	3	10274.
350°C	RTL	1.185	129	108800.
	DTL	.967	19	19600.
	LIN.	.069	4	58309.

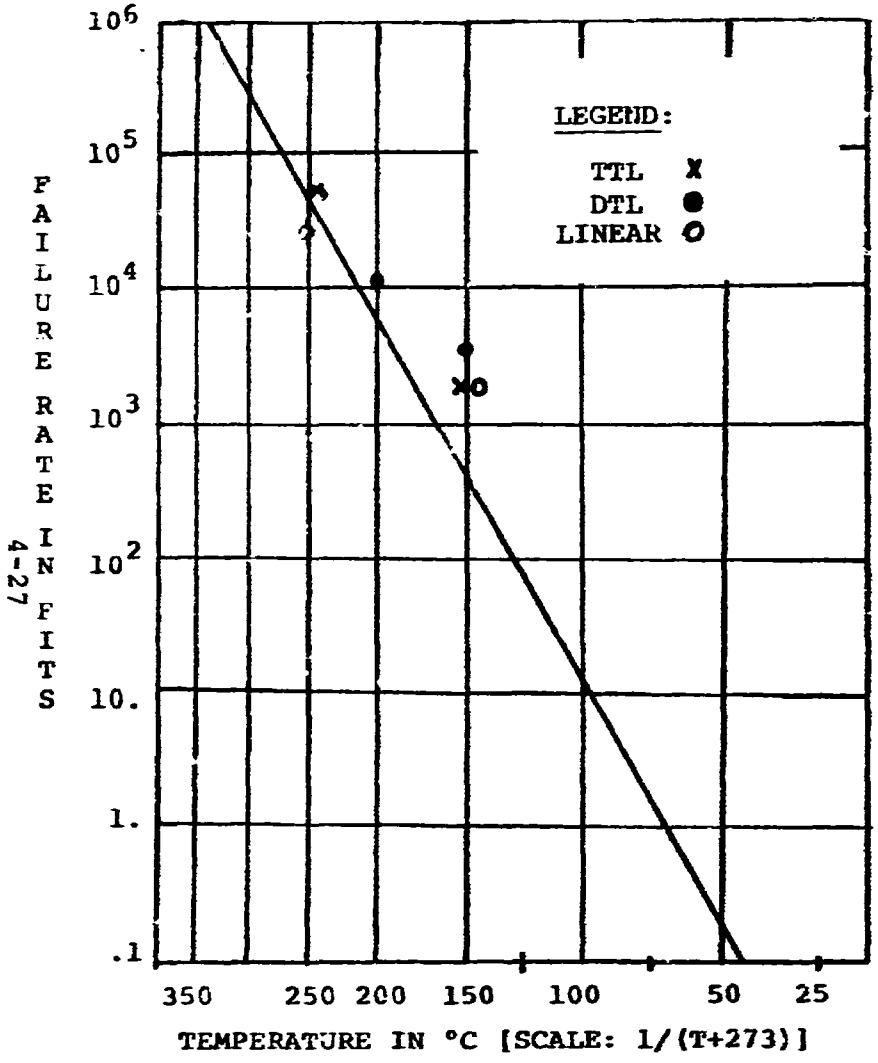


FIGURE 4-8. FUNCTION AND LOGIC TYPE CORRELATION FOR ALUMINUM METAL/GOLD WIRE SYSTEM (CLASS C)

TABLE 4-13. ALUMINUM METAL/GOLD WIRE FUNCTION AND LOGIC TYPE DATA (CLASS C)

TEMP	LOGIC TYPE	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
150°C	DTL	10.886	40	3674.
	TTL	4.962	10	2015.
	LIN.	2.88	6	2083.
175°C	TTL	.282	0	(<3546.)
200°C	DTL	.758	9	11900.
250°C	TTL	.095	6	63150.
	DTL	.22	7	31800.

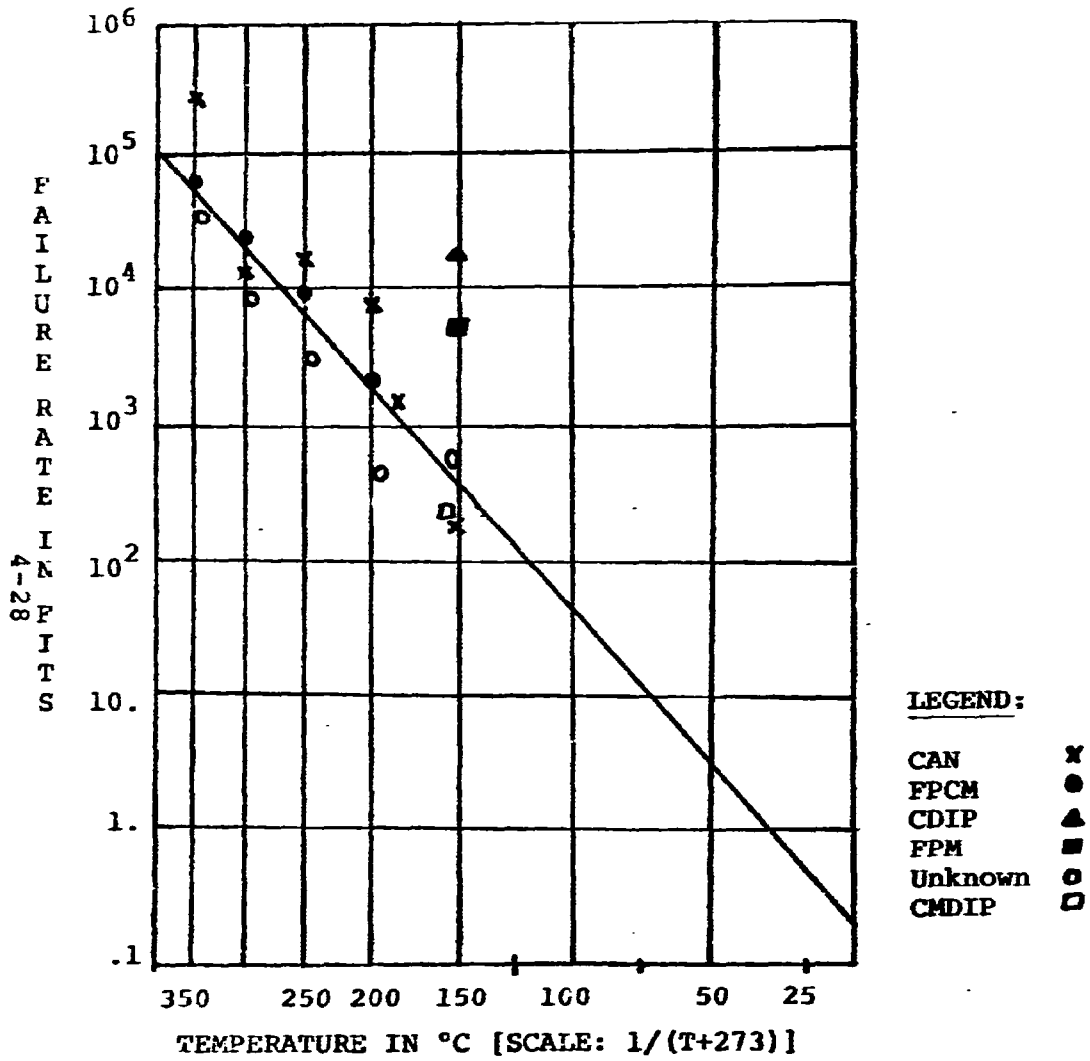


FIGURE 4-9. PACKAGE TYPE CORRELATION FOR ALUMINUM METAL/ALUMINUM WIRE SYSTEM (CLASS C)

TABLE 4-14. ALUMINUM METAL/ALUMINUM WIRE PACKAGE TYPE DATA

QUALITY CLASS	TEMP	PACKAGE TYPE	STOPAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
C	125°C	SDIP	.4	0	(<2500.)
	150°C	CAN	22.267	3	135.
		CMDIP	4.633	1	216.
		CDIP	.052	1	19231.
		SDIP	.192	0	(<5208.)
		FPCM	5.614	0	(<178.)
		FPM	.16	1	6250.
		FPG	.395	0	(<2532.)
		Unknown	48.293	24	497.
	175°C	CAN	5.855	8	1366.
		CDIP	.434	0	(<2304.)
	180°C	CAN	.069	0	(<14493.)
		FPCM	.11	0	(<9091.)
		Unknown	7.89	0	(<127.)
	200°C	CAN	1.165	9	7725.
		FPCM	2.944	6	2038.
		Unknown	4.879	2	410.
	250°C	CAN	.701	12	17126.
		FPCM	.912	9	9868.
		Unknown	1.825	5	2740.
	300°C	CAN	1.132	16	14134.
		FPCM	1.362	33	24229.
		Unknown	1.454	13	8938.
	350°C	CAN	.213	58	271790.
		FPCM	.38	27	71053.
		Unknown	1.628	67	41165.

QUALITY CLASS	TEMP	PACKAGE TYPE	STORAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
D	100°C	CMDIP	.01	0	(<100000.)
	125°C	CAN	2.078	1	481.
		CDIP	.402	1	2487.
		FPCM	.473	3	6349.
	150°C	CDIP	21.036	21	996.
		EDIP	1.124	0	(<890.)
		FPCM	16.348	18	1101.
		CAN	24.471	22	899.
		CMDIP	.255	0	(<3921.)
		FPM	4.512	0	(<222.)
		PDIP	.627	3	4875.
		Unknown	.725	1	1379.
	175°C	CAN	.274	3	10949.
		FPCM	.923	5	5419.
		CDIP	.156	1	6410.
		PDIP	.290	0	(<3448.)
	180°C	FPCM	.205	0	(<4878.)
	200°C	CDIP	.26	1	3837.
		FPCM	6.211	2	322.
	300°C	CAN	.352	22	62553.
		FPCM	.277	5	18054.
		CDIP	.291	25	89126.
	350°C	CAN	.041	29	710784.

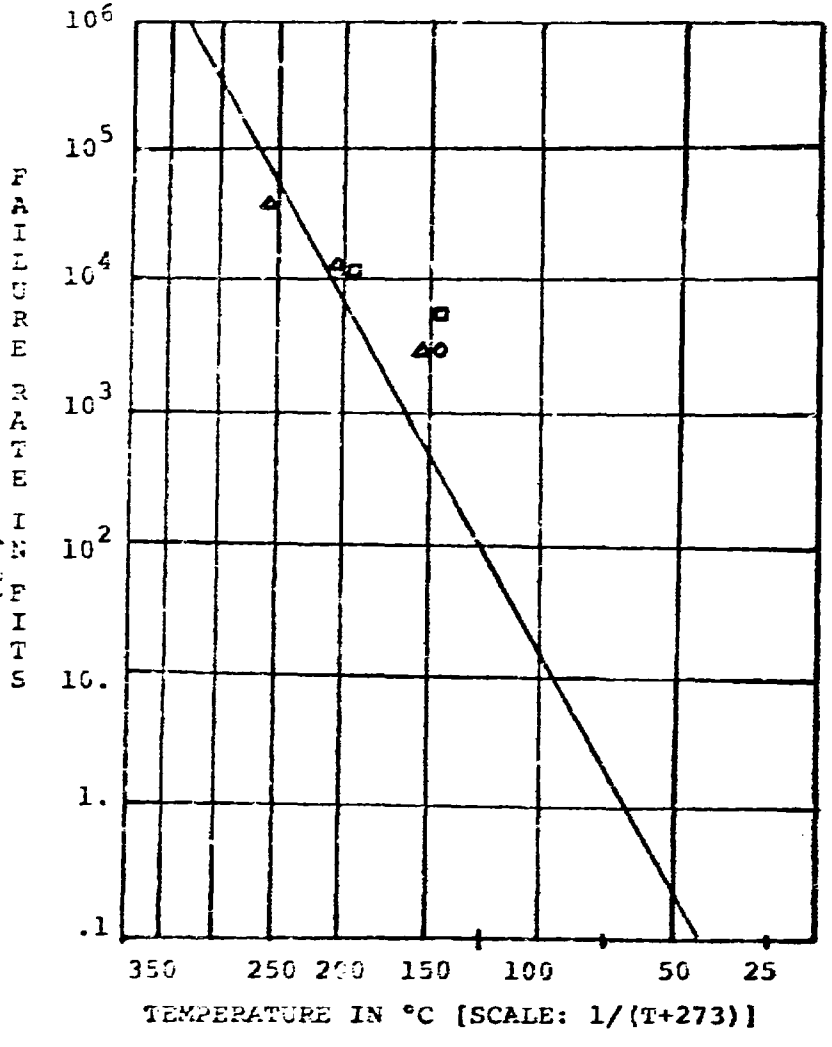


FIGURE 4-10. PACKAGE TYPE CORRELATION FOR ALUMINUM METAL/GOLD WIRE SYSTEM (CLASS C)

TABLE 4-15. ALUMINUM METAL/GOLD WIRE PACKAGE TYPE DATA

QUALITY CLASS	TEMP	PACKAGE TYPE	STORAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
C	150°C	FPCM	.08	0	(<12500.)
		FPG	1.018	3	2947.
		CMDIP	.04	0	(<25000.)
		SDIP	.326	2	6135.
		EDIP	.018	0	(<55000.)
		Unknown	17.246	51	2957.
	175°C	FPG	.282	0	(<3546.)
	200°C	SDIP	.188	2	10638.
		FPG	.57	7	12281.
	250°C	FPG	.315	13	41270.
D	125°C	SDIP	.307	0	(<3257.)
	150°C	FPCM	.129	0	(<7752.)
		PDIP	.265	4	15079.
		SDIP	2.355	9	3822.
		CDIP	3.235	6	1855.
		EDIP	14.493	14	966.
		CAN	.272	1	3676.
		FPM	.085	1	11765.
		Unknown	.077	0	(<12987.)
	180°C	FPM	.086	7	81112.
	200°C	FPM	.119	40	336417.
	250°C	FPM	.068	99	1462000.

4.4.9 Die Attach Method

The data analyzed covered three die attach methods: eutectic alloy, glass frit, and epoxy mounts. However, over 99 percent of the data was on eutectic alloy mounts.

Only 53,000 hours of data was available on epoxy mounts and no suitable statistics could be calculated.

For glass frit mounts some data was available for devices with all-aluminum systems. For Class D devices at 150°C, 6.11 million hours of non-operating time with 4 failures showed a slightly lower failure rate than the eutectic alloy mounts at that temperature. Also for Class D devices at 300°C, 0.17 million hours of non-operating time with 4 failures again showed a lower failure rate than the eutectic alloy mounts. Table 4-16 presents this data for Class C and D devices.

More non-operating time on epoxy and glass frit mounts will be required to determine if the material or the process affects the device storage reliability.

4.4.10 Glassivation

Sixteen percent of the data analyzed indicated that the devices were protected with a glassivation layer. Most of the data was available for Class D devices of the all-aluminum system and is presented in Table 4-17. This data shows glassivated devices with a slightly higher failure rate at 150° and 175°C than non-glassivated devices and a significantly lower failure rate at 300°C. Data for Class D devices with aluminum metal/gold wire systems at 150°C shows glassivated devices with a higher failure rate by a factor of 4 over non-glassivated devices.

As a result of this scatter, no glassivation effect on storage reliability can be determined at this time.

TABLE 4-16. ALUMINUM METAL/ALUMINUM WIRE DIE ATTACH DATA

QUALITY CLASS	TEMP	DIE ATTACH	STORAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
C	150°C	ALLOY	74.259	29	391.
		EPOXY	.044	0	(<22700.)
D	150°C	ALLOY	51.907	50	963.
		GLASS	6.114	4	654.
	300°C	ALLOY	.749	48	64073.
		GLASS	.17	4	23500.

TABLE 4-17. ALUMINUM METAL/ALUMINUM WIRE GLASSIVATION DATA

TEMP	GLASSIVATION	STORAGE HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
100°C	YES	.01	0	(<100000.)
125°C	YES	2.953	5	1693.
150°C	YES	14.186	30	2115.
	NO	41.514	24	578.
175°C	YES	1.203	7	5820.
	NO	.44	2	4545.
180°C	YES	.205	0	(<4878.)
200°C	YES	.253	0	(<3952.)
	NO	6.218	3	482.
300°C	YES	.687	16	23300.
	NO	.233	36	155000.
350°C	NO	.041	29	711000.

4.4.11 Application Environment Complexity Factor (C_2)

The model assumption that the temperature effect and application environment effect are additive allows a direct calculation of the application environment complexity factor, C_2. The failure rate is defined as:

$$\lambda = [\Pi_L \Pi_Q \Pi_T C_1 + \Pi_L \Pi_Q \Pi_E C_2] \times 10^{-6}$$

For Class A all-aluminum system, the failure rate at 25° to 30°C was calculated as .00085 per million hours. Substituting the values for Π_L, Π_Q, Π_T, C_1, and Π_E gives a C_2 factor of approximately 0.00074. The following comparison of the model results with the other quality class data was made as shown in Table 4-18.

For the aluminum metallization/gold wire system, the same calculations were performed using the data collected for quality Class B giving an application environment complexity factor, C_2, of 0.00872. This yielded the results in Table 4-19.

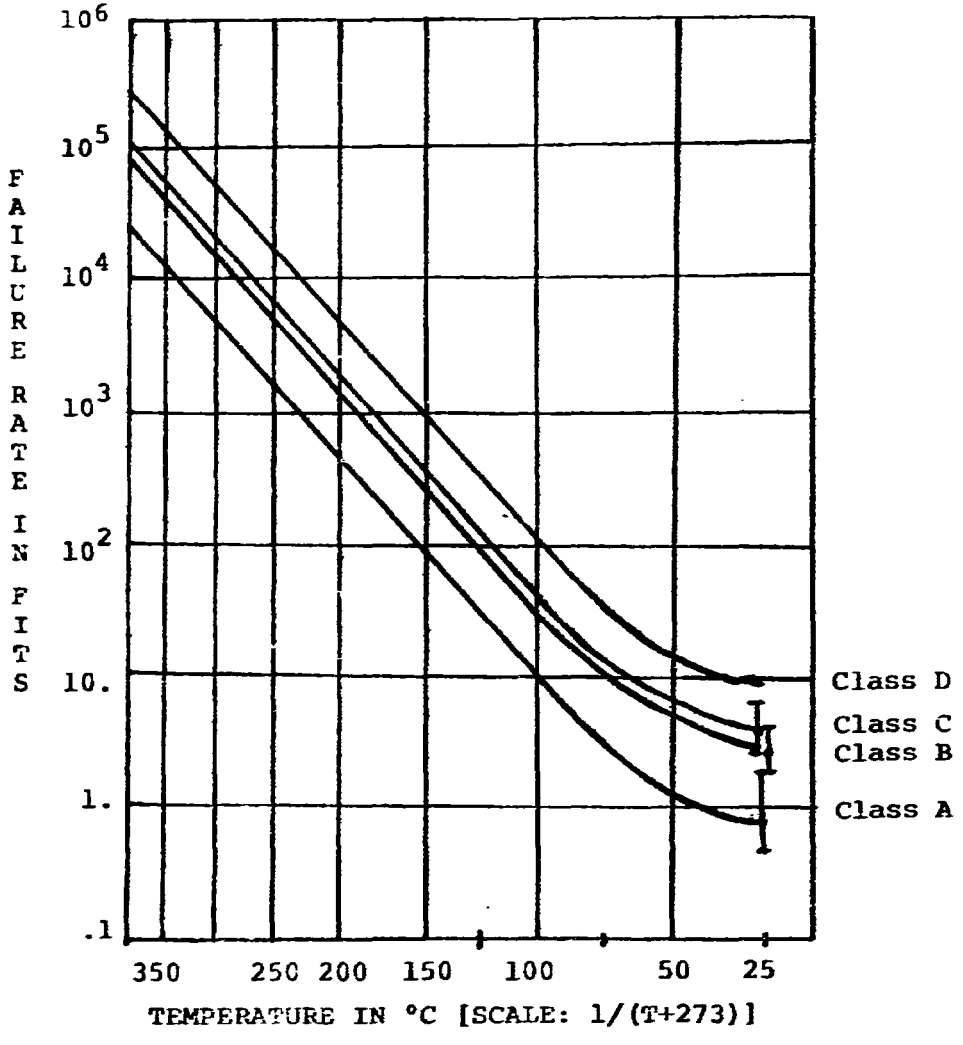
The resulting models for the two metallization systems are depicted in Figures 4-11 and 4-12.

TABLE 4-18. ALUMINUM METALLIZATION/ALUMINUM WIRE FAILURE RATE MODEL RESULTS (Failures per billion hours)

QUALITY LEVEL	PREDICTION MODEL	DIGITAL DATA	LINEAR DATA	COMBINED DATA
Class A	.875	.85	-	.85
Class B	3.06	2.79	4.46	3.30
Class C	3.94	3.8	-	3.8
Class D	9.84	(<217.)	-	(<217.)

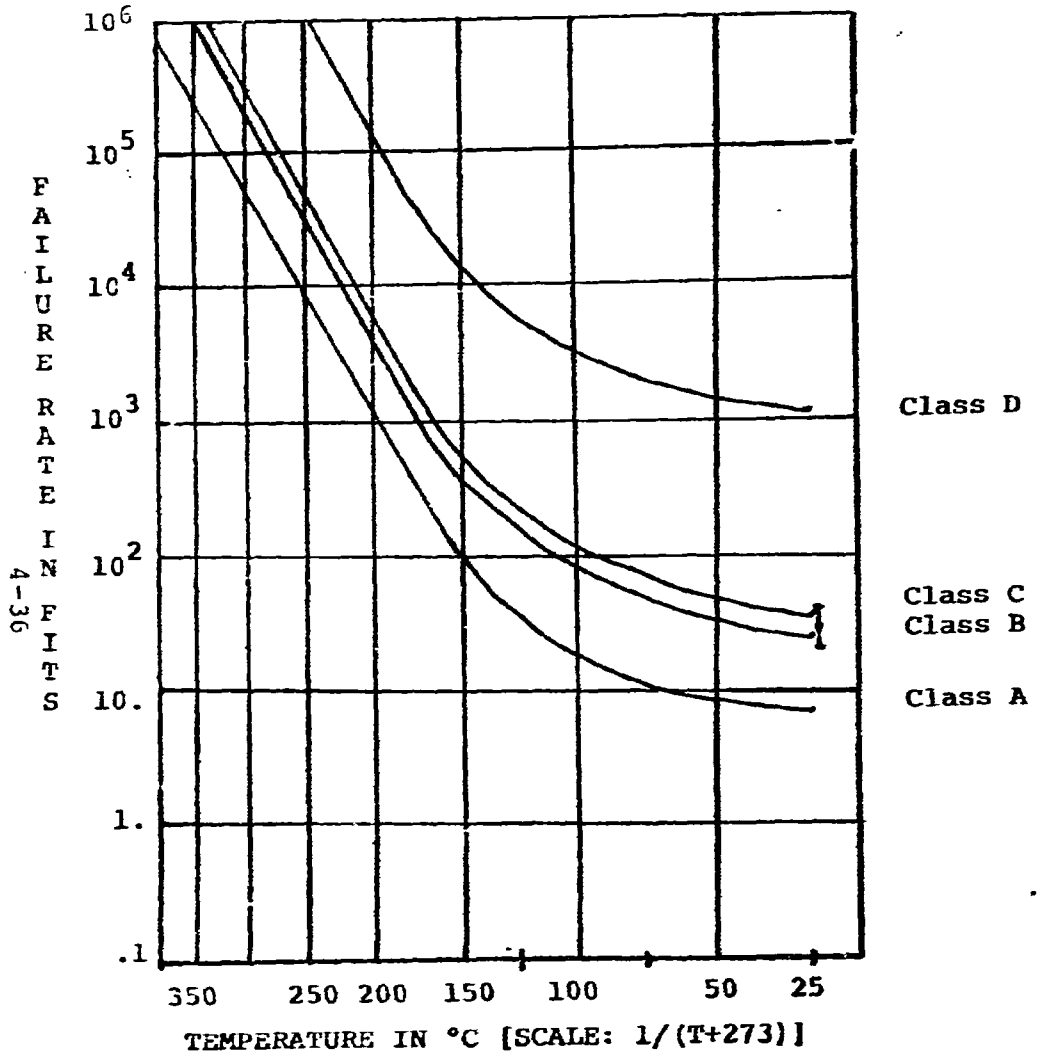
TABLE 4-19. ALUMINUM METALLIZATION/GOLD WIRE FAILURE RATE MODEL RESULTS (Failures per billion hours)

QUALITY LEVEL	PREDICTION MODEL	DIGITAL DATA	LINEAR DATA	COMBINED +DATA
Class A	8.7	-	-	-
Class B	30.5	30.0	53.0	31.0
Class C	39.3	-	-	-
Class D	1177.7	(<3731.)	-	(<3731.)



$$\lambda = \Pi_L \Pi_Q [\Pi_T C_1 + \Pi_E C_2] \times 10^{-6}$$

FIGURE 4-11. MONOLITHIC BIPOLAR DIGITAL AND LINEAR (SSI/MSI) FAILURE RATE PREDICTION (ALUMINUM METAL/ALUMINUM WIRE SYSTEM)



$$\lambda = \pi_L \pi_Q [\pi_T C_1 + \pi_E C_2] \times 10^{-6}$$

FIGURE 4-12. MONOLITHIC BIPOLAR DIGITAL AND LINEAR (SSI/MSI) FAILURE RATE PREDICTION (ALUMINUM METAL/GOLD WIRE SYSTEM)

4.5 Source Data Discussion

Where identified, the real time data collected represented up to eight years storage durations. Tables 4-20 through 4-29 give the data by source and details are presented below.

4.5.1 Source A Data

The data under Source A includes over 9.5 billion storage hours for digital devices and 770 million storage hours for linear devices representing numerous missile and space programs. Twenty one failure were reported including lifted ball bonds due to intermetallics and Kirkendall voiding, metal corrosion, cracked dies, oxide defects and contamination. The data represents Class A, B, and C quality level devices. No details were available on storage environments or durations.

4.5.2 Source B Data

The storage data under Source B actually represents standby data in an orbiting satellite environment. No failures were indicated in 30 million hours. The devices were classified as approximately Class A devices since it was a space application.

4.5.3 Source D Data

The storage data under Source D represents lot samples placed in storage for three to four years. These devices have been tested approximately every 6 months and critical parameters have been recorded. The storage has been in an environmentally controlled facility. Evaluation of parameter changes indicated no significant trends. Out of 350 digital devices and 210 linear devices, no failures have been reported.

4.5.4 Source G Data

The storage data under Source G includes field data from four missile programs and one laboratory environment test. The date of the data sources range from 1967 thru 1970 and represents the only identifiable data on monolithic digital devices with aluminum metallization and gold wires (Al/Au) and on devices with gold metallization and gold wires (Au/Au).

Out of 2.7 billion part storage hours, 83 failures were reported for the Al/Au devices. No failure modes or mechanisms were provided other than the fact that the failures were catastrophic and not drift related. More recent data is available on Al/Au hybrid devices showing the same relatively high failure rate with wire bonds being the major problem (see Section 2.3).

Out of 290 million part storage hours, two failures were reported for Al/Al devices but no failure details were available.

No failures were reported in 18 million part storage hours for the Au/Au devices.

Storage durations for Al/Al devices indicated 2.4 years, and for Au/Au devices, 4 years. No storage durations were available on the Al/Au devices.

4.5.5 Source H Data

The storage data under Source H represents a special parts procurement and storage program. Parts are procured to the highest specification available from the vendor. The procuring agency then performs quality sampling on each lot including construction analysis and puts the device through an extensive rescreening approximating MIL-STD-883 Class A requirements. Under this procedure, 47,340 devices have been rejected and sent back to vendors out of 324,319 parts procured or an average of 14.6% rejects.

The devices passing the screens are placed in airtight storage tanks under controlled temperature and humidity conditions. The interior atmosphere of the tank contains nitrogen.

Samples from each lot are stored separately under identical conditions as control groups. The control groups are tested approximately three times a year. Parameter trends are evaluated from these tests. The main portion of each lot is not tested until required for program use or if control

group parameters are drifting significantly. At this time, no significant drifts have been indicated.

Currently 118,467 monolithic digital & linear bipolar devices have been stored and tested. Ages of these devices range from one month to 8 years with an average of 1.5 years. 118 failures have been reported in these devices, however no failure analysis is available. One group of devices was removed from the analysis.

The data group removed was not considered representative of the general part class since all failures in the devices were related to a specific vendor's process. The group consisted of 12,774 devices stored for an average time of 1.3 years. Thirty one devices were reported failed after the storage period. Failure mechanisms were identical for all devices. The clearance of the interconnect wire to the chip was insufficient. After storage the wire contacted the chip periphery and shorted the device.

4.5.6 Source I Data

The storage data under Source I represents a special test program in 1974-75 to evaluate dormancy and cycling effects on microcircuits.

One thousand IC's were tested for 18 months with the following test profile:

Group	Profile
1	160 units, 2 days off, 1 hour on
2	160 units, 4 days off, 1 hour on
3	160 units, 7 days off, 1 hour on
4	160 units, 9 days off, 1 hour on
5	160 units, 12 days off, 1 hour on
6	200 units, control group, continuously operating

No failures were recorded in the SSI/MSI TTL devices tested.

4.5.7 Source J Data

The storage data under Source J represents field data from two warhead programs. Devices were procured under captive line provisions and are approximately equivalent to MIL-STD-883 Class A specifications. Of the 504 million part storage hours, no failures were reported. Storage durations ranged up to two years.

4.5.8 Source K Data

The storage data under Source K represents SSI RTL devices stored in an environmentally controlled area for eight years (1967 thru 1975). Three failures were recorded in the 10,027 devices all of which were analyzed as resulting from defects in the oxide.

Parameter analysis was performed on 2573 of these devices and compared with those measurements in 1967 to attempt to identify any trends over long term storage. The analysis concluded: "Parameter drift trends proved negligible in the resistance and transistor leakage characteristics. Transistor gain was the only parameter that exhibited a significant loss of performance during the eight years of storage, This is the one parameter that may have to be controlled to obtain a 10-20 year shelf life on these RTL devices."

Of the parts which showed degradation, the most significant performance losses were in those devices whose original performance was more than one standard deviation below the 1967 mean. The loss of performance was significant enough to class 24 parts as "incipient failures." There are parts whose performance has degraded near specification limits and could fall out of spec within the next few years of storage.

The shelf-life drift observed was attributed to one or a combination of following mechanisms:

1) Changes in the gold doping process, which is used to control the "parasitic transistor" condition, as well as to increase part switching speed.

2) Growth of a "parasitic transistor" condition due to migration of contaminants, or to changes in gold doping process.

4.5.9 Missile H Data

Missile H data represents field data from a recent army missile program fielded in the 1970's. The major item in which the devices were assembled was subjected to operating times at high and low temperatures, shock and vibration. The missiles were transported overseas and stored for various lengths of time. No tests were run until the missiles were removed from storage and returned to the states. Storage durations varied from 6 months to 6 years with an average time of 1.8 years. Storage environments included cannister time in a controlled environment, cannister time subject to outside elements and missile time on pallets and on launchers. A number of samples were also run through road tests under field conditions.

Four failures have been reported in 1.9 billion part storage hours. No analysis of the failures is available.

The devices include SSI and MSI TTL & SSI Linear devices and were procured to better than MIL-STD-883 Class C specifications. The user performed sample construction analysis on the devices and screened the parts to better than MIL-STD-883 Class B specifications.

4.5.10 Missile I Data

Missile I data consists of 2,070 missiles stored for periods from 1 month to 40 months for an average storage period of 14 months. Approximately 80 percent of the missiles were stored in the U. S. depots while the remainder were stored at various bases around the country.

Eight failures have been reported in 1.6 billion part storage hours. No analysis of the failures is available. The devices include SSI and MSI TTL and SSI linear devices which were procured to MIL-STD-883 Class B specifications.

TABLE 4-20. SOURCE A DATA (FIELD & TEST)

FUNCTION OR LOGIC TYPE	COM-PLEXITY	QUALITY LEVEL	METAL/ WIRE	NUMBER DEVICES	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
DIG.	-	A	-	-	5328.2	5	0.9
DIG.	-	B	-	-	2269.7	5	2.2
DIG.	-	C	-	-	1952.9	8	4.1
LIN.	-	A	-	-	535.5	1	1.87
LIN.	-	B	-	-	235.5	2	8.49

TABLE 4-21. SOURCE B FIELD DATA

FUNCTION OR LOGIC TYPE	COM-PLEXITY	QUALITY LEVEL	METAL/ WIRE	NUMBER DEVICES	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
DIG.	-	A	-	7903	30.2	0	(<33.1)

TABLE 4-22. SOURCE D SPECIAL TEST DATA

FUNCTION OR LOGIC TYPE	COM-PLEXITY	QUALITY LEVEL	METAL/ WIRE	NUMBER DEVICES	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
TTL	SSI	B	Al/Al	30	.8	0	(<1250.)
TTL	SSI	B	Al/Al	20	.7	0	(<1429.)
TTL	SSI	B	Al/Al	30	.7	0	(<1429.)
TTL	SSI	B	Al/Al	10	.3	0	(<3333.)
TTL	SSI	B	Al/Al	10	.3	0	(<3333.)
TTL	SSI	B	Al/Al	10	.3	0	(<3333.)
TTL	SSI	B	Al/Al	10	.3	0	(<3333.)
TTL	SSI	B	Al/Al	5	.1	0	(<10000.)
TTL	SSI	B	Al/Al	5	.1	0	(<10000.)
TTL	SSI	B	Al/Al	5	.1	0	(<10000.)
TTL	SSI	B	Al/Al	30	.8	0	(<1250.)
TTL	SSI	B	Al/Al	20	.5	0	(<2000.)
TTL	SSI	B	Al/Al	20	.5	0	(<2000.)
TTL	SSI	B	Al/Al	5	.1	0	(<10000.)
TTL	MSI	B	Al/Al	5	.1	0	(<10000.)
TTL	SSI	B	Al/Al	10	.2	0	(<5000.)
TTL	SSI	B	Al/Al	10	.2	0	(<5000.)
TTL	SSI	B	Al/Al	5	.1	0	(<10000.)
TTL	SSI	B	Al/Al	5	.1	0	(<10000.)
TTL	SSI	B	Al/Al	30	.8	0	(<1250.)
TTL	SSI	B	Al/Al	20	.5	0	(<2000.)
TTL	SSI	B	Al/Al	20	.5	0	(<2000.)
TTL	SSI	B	Al/Al	5	.1	0	(<10000.)
TTL	MSI	B	Al/Al	5	.1	0	(<10000.)
TTL	SSI	B	Al/Al	10	.2	0	(<5000.)
TTL	SSI	B	Al/Al	10	.2	0	(<5000.)
TTL	SSI	B	Al/Al	5	.1	0	(<10000.)
OP AMP	SSI	B	Al/Al	40	1.2	0	(<837.)
OP AMP	SSI	B	Al/Al	110	3.7	0	(<268.)
OP AMP	SSI	B	Al/Al	10	.4	0	(<2890.)
OP AMP	SSI	B	Al/Al	10	.2	0	(<4484.)
OP AMP	SSI	B	Al/Al	40	.9	0	(<1157.)

TABLE 4-23. SOURCE G FIELD DATA

FUNCTION OR LOGIC TYPE	COM-PLEXITY	QUALITY LEVEL	METAL/ WIRE	NUMBER DEVICES	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
TTL	MSI	B	Al/Au	-	3.6	0	(<277.)
DTL	SSI	B	Al/Au	-	1240.	49	39.5
DTL	SSI	B	Al/Au	-	119.	5	42.0
TTL	SSI	D	Al/Au	-	.3	0	(<3333.)
CML	SSI	B	Al/Au	-	16.2	0	(<62.)
RTL	SSI	B	Al/Au	-	15.3	1	65.3
RTL	SSI	B	Al/Au	-	1210.	22	18.2
DTL	MSI	B	Al/Al	-	138.	2	14.5
DTL	SSI	C	Al/Al	-	150.	0	(<6.6)
RTL	SSI	D	Al/Al	216	4.6	0	(<217.)
RCTL	SSI	B	Au/Au	-	.4	0	(<2500.)
RCTL	SSI	C	Au/Au	55	1.9	0	(<518.)
RCTL	SSI	C	Au/Au	23	.8	0	(<1244.)
TCTL	SSI	C	Au/Au	10	.4	0	(<286.)
RCTL	SSI	C	Au/Au	41	1.4	0	(<694.)
RCTL	SSI	C	Au/Au	53	1.9	0	(<538.)
RCTL	SSI	C	Au/Au	3	.1	0	(<9524.)
RCTL	MSI	C	Au/Au	63	2.2	0	(<455.)
RCTL	SSI	D	Au/Au	55	1.9	0	(<518.)
RCTL	SSI	D	Au/Au	23	.8	0	(<1244.)
RCTL	SSI	D	Au/Au	41	1.4	0	(<699.)
RCTL	SSI	D	Au/Au	53	1.9	0	(<540.)
RCTL	SSI	D	Au/Au	10	.4	0	(<2857.)
RCTL	SSI	D	Au/Au	3	.1	0	(<9524.)
RCTL	MSI	D	Au/Au	63	2.2	0	(<455.)
AMP FAMILY	-	B	Al/Au	-	114.	6	52.6

TABLE 4-24. SOURCE H SPECIAL TEST DATA

FUNCTION OR LOGIC TYPE	COM-PLEXITY	QUALITY LEVEL	METAL/ WIRE	NUMBER DEVICES	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
DTL	SSI	B-A*	Al/Al	517	5.9	0	(<169.5)
DTL	SSI	B-A*	Al/Al	22548	346.4	4	11.5
DTL	SSI	B-A*	Al/Al	17643	252.9	0	(<3.95)
DTL	SSI	B-A*	Al/Al	11852	170.1	25	147.0
DTL	SSI	B-A*	Al/Al	3015	29.7	4**	134.7
DTL	SSI	B-A*	Al/Al	2603	41.0	2**	48.8
DTL	SSI	B-A*	Al/Al	963	14.4	2**	13.9
DTL	SSI	B-A*	Al/Al	1597	16.7	1**	59.9
DTL	SSI	B-A*	Al/Al	4596	44.4	22**	495.5
DTL	MSI	B-A*	Al/Al	175	1.0	0	(<1000.)
DTL	MSI	B-A*	Al/Al	313	1.0	0	(<1000.)
DTL	MSI	B-A*	Al/Al	413	4.5	2	444.4
DTL	MSI	B-A*	Al/Al	138	1.9	0	(<526.3)
DTL	MSI	B-A*	Al/Au	63	0.2	30	150000.
RTL	SSI	B-A*	Al/Al	846	12.8	0	(<78.1)
RTL	SSI	B-A*	Al/Al	4454	52.3	0	(<19.1)
RTL	SSI	B-A*	Al/Al	1215	22.5	0	(<44.4)
RTL	SSI	B-A*	Al/Al	982	12.4	0	(<80.6)
RTL	SSI	B-A*	Al/Al	5172	90.1	0	(<11.1)
TTL	SSI	B-A*	Al/Al	4086	41.1	0	(<24.3)
TTL	SSI	B-A*	Al/Al	3835	42.7	0	(<23.4)
TTL	SSI	B-A*	Al/Al	329	4.7	0	(<212.8)
TTL	SSI	B-A*	Al/Al	714	7.0	2	285.7
TTL	SSI	B-A*	Al/Al	1998	12.6	0	(<79.4)
TTL	SSI	B-A*	Al/Al	2277	16.0	1	62.5
TTL	SSI	B-A*	Al/Al	560	3.6	0	(<277.8)
TTL	SSI	B-A*	Al/Al	1572	9.5	1	105.3
TTL	SSI	B-A*	Al/Al	39	.1	0	(<10000.)
TTL	SSI	B-A*	Al/Al	373	2.7	0	(<370.4)
TTL	SSI	B-A*	Al/Al	416	3.3	0	(<303.0)
TTL	SSI	B-A*	Al/Al	522	3.9	0	(<256.4)
TTL	SSI	B-A*	Al/Al	133	.6	0	(<1666.7)
TTL	SSI	B-A*	Al/Al	374	2.3	0	(<434.8)
TTL	MSI	B-A*	Al/Al	457	1.3	2	1538.5
TTL	MSI	B-A*	Al/Al	56	.4	0	(<2500.)
TTL-PROM	MSI	B-A*	Al/Al	37	.6	30	50000.
DC AMP	SSI	B-A*	Al/Al	2666	57.2	0	(<17.5)
OP AMP	SSI	B-A*	Al/Al	4948	80.3	9	112.1
DUAL COMP	SSI	B-A*	Al/Al	7521	88.9	1	11.2
LIN.	SSI	B-A*	Al/Al	1371	22.0	1	45.5
DC AMP	SSI	B-A*	Al/Al	1285	9.0	0	(<111.1)
VOLT REG	SSI	B-A*	Al/Al	439	6.8	0	(<147.1)
VOLT COMP	SSI	B-A*	Al/Al	611	5.7	0	(<175.4)
OP AMP	SSI	B-A*	Al/Al	543	4.6	0	(<217.4)
LIN.	SSI	B-A*	Al/Al	314	2.9	1	344.8
OP AMP	SSI	B-A*	Al/Al	90	2.8	3	(<1071.4)
VOLT COMP	SSI	B-A*	Al/Al	159	4.4	0	(<227.3)
OP AMP	SSI	B-A*	Al/Al	321	1.7	0	(<588.2)
LIN.	SSI	B-A*	Al/Al	1316	5.1	6	1176.5

*Special Testing - See Text
**Vendor Peculiar Problem - See Text

TABLE 4-25. SOURCE I SPECIAL TEST DATA*

LOGIC TYPE	COM-PLEXITY	QUALITY LEVEL	METAL/ WIRE	NUMBER DEVICES	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
TTL	SSI	B	Al/Al	200	2.6	0	(<385.)
TTL	MSI	B	Al/Al	200	2.6	0	(<385.)
TTL	MSI	B	Al/Al	200	2.6	0	(<385.)
TTL	SSI	B	Al/Al	200	2.6	0	(<385.)

*Cycled.

TABLE 4-26. SOURCE J FIELD DATA

LOGIC TYPE	COM-PLEXITY	QUALITY LEVEL	METAL/ WIRE	NUMBER DEVICES	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
DIG.	-	A	Al/Al	7700	31.	0	(<32.3)
DIG.	-	A	Al/Al	-	472.	0	(<2.1)

TABLE 4-27. SOURCE K SPECIAL TEST DATA

LOGIC TYPE	COM-PLEXITY	QUALITY LEVEL	METAL/ WIRE	NUMBER DEVICES	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
RTL	SSI	B	Al/Al	1250	87.6	0	(<11.4)
RTL	SSI	B	Al/Al	2382	166.9	1	6.0
RTL	SSI	B	Al/Al	1002	70.2	0	(<14.2)
RTL	SSI	B	Al/Al	949	66.5	2	30.1
RTL	SSI	B	Al/Al	1002	70.2	0	(<14.2)
RTL	SSI	B	Al/Al	450	31.5	0	(<31.7)
RTL	SSI	B	Al/Al	2992	209.7	0	(<4.8)

TABLE 4-28. MISSILE H FIELD DATA

FUNCTION OR LOGIC TYPE	COM-PLEXITY	QUALITY LEVEL	METAL/ WIRE	NUMBER DEVICES	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
TTL	SSI	B	Al/Al	5355	85.1	0	(<11.8)
TTL	SSI	B	Al/Al	7497	119.1	1	8.4
TTL	MSI	B	Al/Al	19278	306.3	0	(<3.3)
TTL	SSI	B	Al/Al	1071	17.0	0	(<58.8)
TTL	SSI	B	Al/Al	7497	119.1	0	(<8.4)
TTL	SSI	B	Al/Al	8568	136.1	0	(<7.3)
OP AMP	SSI	B	Al/Al	37485	597.6	1	1.67
DC AMP	SSI	B	Al/Al	14994	239.0	1	4.18
DC AMP	SSI	B	Al/Al	18207	290.3	1	3.44

TABLE 4-29. MISSILE I FIELD DATA

FUNCTION OR LOGIC TYPE	COM-PLEXITY	QUALITY LEVEL	METAL/ WIRE	NUMBER DEVICES	PART HOURS X 10^6	NUMBER FAILED	FAILURE RATE IN FITS
TTL	SSI	B	Al/Al	16560	164.7	1	6.1
TTL	MSI	B	Al/Al	4140	41.2	0	(<24.3)
TTL	MSI	B	Al/Al	26910	267.7	1	3.7
TTL	SSI	B	Al/Al	16560	164.7	0	(<6.1)
TTL	SSI	B	Al/Al	10350	103.0	0	(<9.7)
OP AMP	SSI	B	Al/Al	51750	514.8	2	3.9
OP AMP	SSI	B	Al/Al	2070	20.6	1	48.5
OP AMP	SSI	B	Al/Al	8280	82.4	2	23.7
DUAL COMP	SSI	B	Al/Al	26910	267.7	1	3.7

SECTION 5

STORAGE FAILURE RATE PREDICTION MODEL

The prediction models presented here apply only to monolithic bipolar digital and linear integrated circuits with complexity ranges of small scale integration and medium scale integration (up to 100 gates). Failure rates prediction of multilayer interconnect devices is not included. Secondary failures caused by abusive voltage conditions or errors in maintenance and trouble shooting procedures are also not included.

The model is similar to that presented in MIL-HDBK-217B for operational failure rate predictions. It assumes that the predominant failures result from two primary use factors: time/temperature phenomena and mechanical stress phenomena (handling, vibration, temperature cycling, etc.). The model therefore is defined as follows:

$$\lambda_s = \lambda_t + \lambda_m$$

where

λ_s = the device storage failure rate

λ_t = the device storage failure rate due to the time/temperature phenomena

λ_m = the device storage failure rate due to mechanical stress phenomena

The time temperature phenomena results in failure mechanisms such as: surface inversion, degradation of bonds between dissimilar metals, corrosion, Kirkendall diffusion, degradation of feed throughs, dielectric degradation at flaws, ohmic contact degradation and junction bridging by diffused aluminum.

The mechanical stress phenomena results in failure mechanisms such as: open bonds, shorted bond wires, cracked chips, metal opens at oxide steps, degradation or bridging of dielectric, die bond separation, lead wire fatigue fracture, seal failure and gross package damage.

Both phenomena are affected by the procurement technique which defines the quality level of the device. Also the maturity of the device design and process affects the failure rate.

The prediction model is therefore broken in to these factors:

$$\lambda_s = [\Pi_L \Pi_Q \Pi_T C_1 + \Pi_L \Pi_Q \Pi_E C_2] \times 10^{-6}$$

or

$$\lambda_s = \Pi_L \Pi_Q [\Pi_T C_1 + \Pi_E C_2] \times 10^{-6}$$

where:

Π_L is the learning factor
Π_Q is the quality level factor
Π_T is the temperature factor
Π_E is the application environment factor
C_1 and C_2 are base failure rates for the time/temperature phenomena and the mechanical stress phenomena respectively

The factors for monolithic bipolar SSI/MSI digital devices with aluminum metallization/aluminum wire systems are defined in Table 5-1 and for devices with aluminum metallization/ gold wire systems in Table 5-2.

The values for the learning factor, Π_L, and application environment factor, Π_E, are used as defined in MIL-HDBK-217B.

The values for the temperature factor, Π_T, are based on an Arrhenius model. For devices with aluminum metallization, aluminum wire systems, the temperature factor is defined as:

$$\Pi_T = 0.1 \exp \left[-6608 \left(\frac{1}{T+273} - \frac{1}{298} \right) \right]$$

where T is the ambient temperature, in degrees centigrade. For devices with aluminum metallization gold wire systems, the temperature factor is defined as:

$$\Pi_T = 0.1 \exp \left[-10502 \left(\frac{1}{T+273} - \frac{1}{298} \right) \right]$$

The π_Q factors represent MIL-STD-883 quality classes and were measured for the all-aluminum devices but are estimated for the gold/aluminum devices.

Models for devices with all gold metallization/interconnection systems and beam lead sealed junction systems are not given at this time due to lack of data.

FIGURE 5-1. MONOLITHIC BIPOLAR SSI/MSI DIGITAL AND LINEAR DEVICE FAILURE RATE PREDICTION MODEL (FOR ALUMINUM METALLIZATION/ALUMINUM WIRE SYSTEM)

$$\lambda_s = \Pi_L \Pi_Q [\Pi_T C_1 + \Pi_E C_2] \times 10^{-6}$$

Π_L (Learning Factor)

(For this interim analysis, assumes MIL-HNBK-217B values.)
Π_L = 10 for 1) a new device in initial production 2) a major change in design or process 3) extended line interruption or change in line personnel. Π_L = 1 otherwise

Π_Q (Quality Factor)

MIL-STD 883 Class	Π_Q
A	1
B	3.5
C	4.5
D	11.25

Π_T (Temperature Factor)

$$\Pi_T = 0.1 \exp\left[-6608\left(\frac{1}{T+273} - \frac{1}{298}\right)\right]$$

Temperature °C	Π_T
25	0.1
30	0.14
40	0.29
50	0.56
100	8.64
125	26.28
150	70.12
170	141.94

Π_E (Application Environment Factor)

(For this interim analysis, assumes MIL-HNBK-217B values.)	
Environment	Π_E
Ground, Benign	0.2
Ground, Fixed	1.0
Ground, Mobile	4.0
Airborn, Inhabited	
Missile Launch	10.0

C_1 (Time/Temperature Base Failure Rate)

C_1 = 0.00135

C_2 (Mechanical Stress Base Failure Rate)

C_2 = 0.00074

FIGURE 5-2. MONOLITHIC BIPOLAR SSI/MSI DIGITAL AND LINEAR DEVICE FAILURE RATE PREDICTION MODEL (FOR ALUMINUM METALLIZATION/GOLD WIRE SYSTEM)

$$\lambda_s = \Pi_L \Pi_Q [\Pi_T C_1 + \Pi_E C_2] \times 10^{-6}$$

Π_L (Learning Factor)

(For this interim analysis, assumes MIL-HNBK-217B values)
Π_L = 10 for 1) a new device in initial production 2) a major change in the design or process 3) extended line interrupt or change in line personnel
Π_L = 1 otherwise

Π_Q (Quality Factor)

MIL-STD-883 Class	Π_Q
A	1
B	3.5
C	4.5
D	135

Π_T (Temperature Factor)

$$\Pi_T = 0.1 \exp\left[-10502\left(\frac{1}{T+273} - \frac{1}{298}\right)\right]$$

Temperature °C	Π_T
25	0.1
30	0.18
40	0.54
50	1.53
100	119.53
125	700.71
150	3332.91
170	10223.86

Π_E (Application Environment Factor)

(For this interim analysis, assumes MIL-HNBK-217B values)	
Environment	Π_E
Ground, Benign	0.2
Ground, Fixed	1.0
Ground, Mobile	4.0
Airborn, Inhabited	
Missile Launch	10.0

C_1 (Time/Temperature Base Failure Rate)

C_1 = 0.000034

C_2 (Mechanical Stress Base Failure Rate)

C_2 = 0.00872

SECTION 6

OPERATIONAL FAILURE RATE ANALYSIS

Two reliability data banks and a reliability prediction model were reviewed for operational failure rate predictions. The prediction model in MIL-HDBK-217B was considered an acceptable source for predicting operational failure rates for standard monolithic, bipolar, digital & linear devices. For some non-standard devices, such as beam lead sealed junction devices, more specific prediction methods may be required. Access to the Reliability Analysis Center and GIDEP data banks can provide specific data on similar non-standard devices for reliability prediction.

6.1 MIL-HDBK 217B Digital IC Model

The prediction model in MIL-HDBK-217B, dated 20 September 1974, for monolithic bipolar digital SSI/MSI devices is presented in Figure 6-1.

The temperature factor, Π_T, is defined as follows:

$$\Pi_T = 0.1 \exp \left[-4794 \left(\frac{1}{T_J + 273} - \frac{1}{298} \right) \right]$$

where T_J is the junction temperature

If the junction temperature is unknown, the following approximation is used:

T_J = ambient T + 10°C, if the number of transistors is less than or equal to 120

T_J = ambient T + 25°C, if the number of transistors is greater than 120

The complexity factors, C_1 and C_2, are defined as follows:

$$C_1 = 1.29 \ (10)^{-3} (N_G)^{0.677}$$

$$C_2 = 3.89 \ (10)^{-3} (N_G)^{0.359}$$

where N_G = number of gates (assume 4 transistors/gate)

FIGURE 6-1. MIL-HDBK-217B OPERATIONAL FAILURE RATE MODEL
MONOLITHIC BIPOLAR DIGITAL SSI/MSI INTEGRATED CIRCUITS
(TTL, DTL, etc. excludes Beam Lead & ECL)

$$\lambda_p = \Pi_L \Pi_Q (\Pi_T C_1 + \Pi_E C_2) \times 10^{-6}$$

Π_L (Learning Factor)

Π_L = 10 for 1) a new device in initial production
2) a major change in design or process
3) extended line interruption or change in line personnel

Π_L = 1 otherwise

Π_Q (Quality Factor)

Quality Level	Π_Q
MIL-M-38510 Class A (JAN)	1
MIL-M-38510 Class B (JAN)	2
MIL-STD-883 Method 5004 Class B	5
Vendor Equiv. MIL-STD-883 Method 5004 Class B	10
MIL-M-35810 Class C (JAN)	16
Commercial Class D	150

C_1 & C_2 (Complexity Factors)

No. Gates	C_1	C_2	No. Gates	C_1	C_2
1	.0013	.0039	46	.017	.015
2	.0021	.0050	48	.018	.016
4	.0033	.0064	50	.018	.016
6	.0043	.0074	52	.019	.016
8	.0053	.0082	54	.019	.016
10	.0061	.0089	56	.020	.017
12	.0069	.0095	58	.020	.017
14	.0077	.010	60	.021	.017
16	.0084	.011	62	.021	.017
18	.0091	.011	64	.022	.017
20	.0098	.011	66	.022	.018
22	.011	.012	68	.022	.018
24	.011	.012	70	.023	.018
26	.012	.013	72	.023	.018
28	.012	.013	74	.024	.018
30	.013	.013	76	.024	.019
32	.014	.014	78	.025	.019
34	.014	.014	80	.025	.019
36	.015	.014	85	.026	.019
38	.015	.014	90	.027	.020
40	.016	.015	95	.028	.020
42	.016	.015	99	.029	.020
44	.017	.015			

Π_T (Temperature Factor)

T_j (°C)	Π_T	T_j (°C)	Π_T	T_j (°C)	Π_T	T_j (°C)	Π_T
25	.10	51	.36	77	1.1	103	2.8
27	.11	53	.40	79	1.2	105	3.0
29	.12	55	.44	81	1.3	110	3.4
31	.14	57	.48	83	1.4	115	4.2
33	.15	59	.52	85	1.5	120	4.9
35	.17	61	.57	87	1.6	125	5.7
37	.19	63	.62	89	1.7	135	7.7
39	.21	65	.67	91	1.9	145	10.
41	.23	67	.73	93	2.0	155	13.
43	.25	69	.79	95	2.1	165	17.
45	.28	71	.86	97	2.3	175	22.
47	.30	73	.93	99	2.5		
49	.33	75	1.0	101	2.6		

Π_E (Environmental Factor)

Environment	Π_E
Ground, Benign	0.2
Space Flight	0.2
Ground, Fixed	1.0
Airborne, Inhabited	4.0
Naval, Sheltered	4.0
Ground, Mobile	4.0
Airborne, Uninhab.	6.0
Naval, Unsheltered	5.0
Satellite or Missile, Launch	10.0

These complexity factors apply to devices in packages containing up to 22 pins. For larger packages the C_1, C_2 values are multiplied by:

No. of Pins	Multiplier
24 to 40	1.1
42 to 64	1.2
>64	1.3

This model applies to all monolithic bipolar digital devices except bipolar beam lead and bipolar ECL. For these devices, a different temperature factor, Π_T, is used and is defined as follows:

$$\Pi_T = 0.1 \exp \left[-8121 \left(\frac{1}{T_J + 273} - \frac{1}{298} \right) \right]$$

where T_J is the junction temperature

Typical temperature factor, Π_T, values for these devices are presented in Table 6-1.

In the 217B model, the learning factor estimates the effect of new production lines with the typical experience relationship in which unit cost decreases and reliability increases with larger production runs.

The quality factor estimates the effect of process control, screening, and quality conformance testing on the device reliability.

The junction temperature factor reflects one of the principle degrading factors for semiconductor devices. The failure rate to temperature relationship is the Arrhenius model which says that the natural log of the basic failure rate is a function of the negative reciporcal of the absolute junction temperature.

Table 6-1.

TEMPERATURE FACTOR VALUES FOR
BIPOLAR BEAM LEAD AND BIPOLAR ECL DIGITAL DEVICES

T_J	π_T
25	.10
35	.24
45	.56
55	1.20
65	2.50
75	5.00
85	9.60
95	18.00
105	32.00
115	56.00
125	94.00
135	155.00
145	250.00
155	390.00
165	610.00
175	920.00

The application environment factor estimates primarily the mechanical stress effects on the device failure rates. These stresses include vibration, shock, acceleration, and temperature cycling.

The complexity factors both for temperature and application environment represent a number of reliability factors. These include the device strength as a function of package size; the number of interconnections; the density of active elements on the chip and resulting metallization runs; and the thermal conduction capability from the chip to external heat sinks.

6.2 MIL-HDBK-217B Linear IC Model

The prediction model in MIL-HDBK-217B, dated 20 September 1974, for monolithic bipolar linear SSI/MSI devices is presented in Figure 6-2.

The temperature factor, Π_T, is defined as follows:

$$\Pi_T = 0.1 \exp\left[-8121\left(\frac{1}{T_J+273} - \frac{1}{298}\right)\right]$$

where T_J is the junction temperature

If the junction temperature is unknown, the following approximation is used:

T_J = ambient T + 10°C, if the number of transistors is less than or equal to 120

T_J = ambient T + 25°C, if the number of transistors is greater than 120

The complexity factors, C_1 and C_2, are defined as follows:

$$C_1 = .00056\ (N_T)^{0.763}$$

$$C_2 = .0026\ (N_T)^{0.547}$$

where N_T = number of transistors

This model applies to all monolithic bipolar linear devices.

In the 217B model, the learning factor estimates the effect of new production lines with the typical experience relationship in which unit cost and reliability decrease with larger production runs.

The quality factor estimates the effect of process control, screening, and quality conformance testing on the device reliability.

The junction temperature factor reflects one of the principle degrading factors for semiconductor devices. The failure rate to temperature relationship is the Arrhenius model which says that the natural log of the basic failure rate is a function of the negative reciprocal of the absolute junction temperature.

FIGURE 6-2. MIL-HDBK-217B OPERATIONAL FAILURE RATE PREDICTION MODEL FOR MONOLITHIC BIPOLAR LINEAR SSI/MSI DEVICES

$$\lambda_p = \Pi_L \Pi_Q (\Pi_T C_1 + \Pi_E C_2) \times 10^{-6}$$

Π_L (Learning Factor)

Π_L = 10 for 1) a new device in initial production
2) a major change in design or process
3) extended line interruption or change in line personnel

Π_L = 1 otherwise

Π_Q (Quality Factor)

Quality Level	Π_Q
MIL-M-38510 Class A (JAN)	1
MIL-M-38510 Class B (JAN)	2
MIL-STD-883 Method 5004 Class B Vendor Equiv.	5
MIL-STD-883 Method 5004 Class B	10
MIL-M-35810 Class C (JAN)	16
Commercial Class D	150

C_1 & C_2 (Complexity Factors)

No. Trans	C_1	C_2	No. Trans	C_1	C_2
4	.0016	.0056	92	.018	.031
8	.0027	.0081	96	.018	.032
12	.0037	.010	100	.019	.032
16	.0046	.012	108	.020	.034
20	.0055	.013	116	.020	.035
24	.0063	.015	124	.022	.036
28	.0071	.016	132	.023	.038
32	.0079	.017	140	.024	.039
36	.0086	.019	148	.025	.040
40	.0093	.020	156	.026	.041
44	.010	.021	164	.027	.043
48	.011	.022	172	.028	.044
52	.011	.023	180	.029	.045
56	.012	.024	188	.030	.046
60	.013	.025	196	.031	.047
64	.014	.025	204	.032	.048
68	.014	.026	220	.034	.050
72	.015	.027	236	.036	.052
76	.015	.028	252	.038	.054
80	.016	.029	268	.040	.056
84	.016	.030	284	.042	.057
88	.017	.030	300	.043	.059

Π_T (Temperature Factor)

T_j (°C)	Π_T	T_j (°C)	Π_T	T_j (°C)	Π_T	T_j (°C)	Π_T
25	.10	51	.89	77	5.7	103	28.
27	.12	53	1.0	79	6.5	105	32.
29	.14	55	1.2	81	7.5	110	42.
31	.17	57	1.4	83	8.5	115	56.
33	.20	59	1.6	85	9.6	120	73.
35	.24	61	1.9	87	11.	125	94.
37	.29	63	2.2	89	12.	135	155.
39	.34	65	2.5	91	14.	145	250.
41	.40	67	2.9	93	16.	155	390.
43	.47	69	3.3	95	18.	165	610.
45	.56	71	3.8	97	20.	175	920.
47	.65	73	4.4	99	23.		
49	.76	75	5.0	101	25.		

Π_E (Environmental Factor)

Environment	Π_E
Ground, Benign	0.2
Space Flight	0.2
Ground, Fixed	1.0
Airborne, Inhabited	4.0
Naval, Sheltered	4.0
Ground, Mobile	4.0
Airborne, Uninhab.	6.0
Naval, Unsheltered	5.0
Satellite or Missile, Launch	10.0

The application environment factor estimates primarily the mechanical stress effects on the device failure rates. These stresses include vibration, shock, acceleration, and temperature cycling.

The complexity factors both for temperature and application environment represent a number of reliability factors. These include the device strength as a function of package size; the number of interconnections; the density of active elements on the chip and resulting metallization runs; and the thermal conduction capability from the chip to external heat sinks.

6.3 Reliability Analysis Center Failure Rate Data Bank

The largest published reliability data bank for microcircuit reliability is maintained by the Reliability Analysis Center (RAC) at Rome Air Development Center. A comparison between data in the RAC data bank and the MIL-HDBK-217B model for bipolar digital devices was made in MDR-1 "Digital Generic Data," 1975. A similar comparison was made for linear devices in MDR-6 "Linear/Interface Data," 1977. This comparison indicated a close correlation between the RAC data and the MIL-HDBK-217B predictions. A sample page from the RAC publication is presented in Figure 6-3. The user requiring an operational failure rate prediction can relate the device and usage with similar devices in the publication. The relationship can include device screen class, operational type, function, application environment, and design and process factors.

6.4 GIDEP Failure Rate Data Bank

The Government-Industry Data Exchange Program (GIDEP) reliability data bank maintained by the Department of the Navy, Fleet Missile Systems Analysis and Evaluation Group, for all services, contains another large source of operational data for bipolar digital microcircuits. A sample page from the GIDEP Summaries of Failure Rate Publication is presented in Figure 6-4.

FIGURE 6-3. SAMPLE OF RAC MICROCIRCUIT GENERIC FAILURE RATES PUBLICATION

TECHNOLOGY: BIPOLAR JUNCTION

OPERATIONAL TYPE: TTL

SCREEN CLASS: B

MICROCIRCUIT GENERIC FAILURE RATES

RELIABILITY ANALYSIS CENTER

LINE NO.	DEVICE FUNCTION	PKGING TYP PINS	METAL SYST METLOGY	INTERCON SYS EM DIE BOND	DATA SRCE	TEST TYPE APP ENV	STRS LVL/ EOP TYPE	NO. TST NO. FLD	PART HOURS	FAILURE CLASSIFICATION PAD, MICRO, MECH, CAUSE ENG. ASSESSMENT	TEST DATE
678	COUNTER DECADE GATES= 27	FPK -H 14 -55/125	AL 1	ALWIRE 14 EUTECTIC	CHK U	TEMP GRNDBEN	CMOTNS 030C	0	1503E1		2/70 7/71
679	COUNTER DECADE GATES= 22	FPK -H 14 -55/125	AL 1	ALWIRE 14 EUTECTIC	REL U	TCVPC GRNDBEN	CMOTNS -055C 072C 241CY2,2863X	0	9830B1		2/70 7/71
680	COUNTER DECADE GATES= 22	FPK -H 14 -55/125	AL 1	ALWIRE 14 EUTECTIC	REL U	TCVPC GRNDBEN	CMOTNS -055C 072C 241CY 83%	0	1752E3		2/70 7/71
681	COUNTER DECADE GATES= 22	FPK -H 14 -55/125	AL 1	ALWIRE 14 EUTECTIC	FLB U	TEMP AIRINHA	CMOTNS 050C	0	508520		9/72 5/73
682	COUNTER DECADE GATES= 54	DIP -H 16 -55/125	AL 1	ALWIRE 16 EUTECTIC	CHK U	TEMP GRNDBEN	CMOTNS 025C 100%	0	4780E0		5/73 9/73
683	COUNTER DECADE GATES= 54	DIP -H 16 -55/125	AL 1	ALWIRE 16 EUTECTIC	REL U	TEMP GRNDBEN	CMOTNS 025C	0	2580E2		5/73 9/73
* 684	DECODER GATES= 18	DIP -H 14 -55/125	AL 1 GLASS	ALWIRE 16 EUTECTIC	CHK U	AIRINHA	COMBIN 050C	1	1130E3	/ 1	1/73 3/74
685								10	1130E3	/10	10/69 1/73
686	DECODER GATES= 18	DIP -H 16 -55/125	AL 1	ALWIRE 16 EUTECTIC	CHK U	TEMP GRNDBEN	CMOTNS 025C 100%	0	407280		5/73 9/73
687	DECODER GATES= 18	DIP -H 16 -55/125	AL 1	ALWIRE 16 EUTECTIC	REL U	TEMP GRNDBEN	CMOTNS 025C	0	2210E2		5/73 9/73
688	DECODER GATES= 18	FPK -H 16 -55/125	AL 1	ALWIRE 16 EUTECTIC	LIFE V	STG LIF	150C	105 0	1050E2		1/74
689	DECODER GATES= 15	FPK -H 16 -55/125	AL 1	ALWIRE 16 EUTECTIC	LIFE V	RNGCNT	125C 100%	176 1	1760F2	/ 1	1/74

* COMBINATION OF SCREEN CLASSES "NONE" TO "B"

FIGURE 6-4. SAMPLE OF GIDEP SUMMARIES OF FAILURE RATE DATA

FAILURE RATE DATA

ACCESS NUMBER	PART CODE	ITEM NUMBER	VENDOR	OBSERVED ENVIRONMENT WITH MODIFIERS	APPLICATION	STRESS LEVEL ES-I-MS	SCN CLS	OBSERVATION PERIOD BEGIN/END	MNT MHRS	NBR. FAIL	NBR. ITEMS	DURATION	UNIT OF MEASURE	60% GROUP CONFIDENCE INTERVAL LOWER MEAN UPPER FAILURE RATE /MILLION
515.1 INTEGRATED-CIRCUITS,FLIP-FLOP (Continued)														LO BOUND 1.056 HO BOUND
FDI-1214	76	PL-948-5I	PHILCO	LAB-LIFE	-	- -	-	1267/1268	-	0	3	8129	HRS	<37.317
FDI-1190	76	84-948J	RAYTHEON	LAB-LIFE-CONT	-	M-M-	-	1267/0568	-	0	3	2516	HRS	<120.561
FDI-1343	76	UA3Y948S1A	FAIRCHILD	LAB-LIFE	-	-M-	-	1267/1269	-	0	3	17184	HRS	<17.652
FDI-1343	76	TFF3243	TRANSITRON	LAB-LIFE	-	M-M-	-	1267/1269	-	0	3	17184	HRS	<17.652
FDI-1214	76	N88268	SIGNETICS	LAB-LIFE	-	M-M-	-	1267/1268	-	0	2	8129	HRS	<55.972
FDI-1343	76	PL9948-51	PHILCO	LAB-LIFE	-	-M-	-	1267/1269	-	0	3	17184	HRS	<17.652
FDI-1190	76	54-948-1F	STEWART-WA	LAB-LIFE-CONT	-	M-M-	-	1267/0568	-	0	3	2516	HRS	<120.561
FDI-1343	76	MC946F	MOTOROLA	LAB-LIFE	-	-M-	-	1267/1269	-	0	3	17184	HRS	<17.652
FDI-1313	6E	28883	PHILCO	LAB-LIFE	-	M-M-	-	/0769	-	0	24	667	HRS	<56.675
FDI-1190	76	TFF-3243	TRANSITRON	LAB-LIFE-CONT	-	M-M-	-	1267/0568	-	0	3	2516	HRS	<120.561
FDI-1367	38	MC1670S	MOTOROLA	LAB-CONT	-	-M-	-	0970/1070	-	0	3	3500	HRS	<86.666
FDI-1214	76	N4948J	RAYTHEON	LAB-LIFE	-	- -	-	1267/1268	-	0	3	8129	HRS	<37.317
FDI-1190	76	U31994851A	FAIRCHILD	LAB-LIFE-CONT	-	M-M-	-	1267/0568	-	0	3	2516	HRS	<120.561
FDI-1214	76	U31994851A	FAIRCHILD	LAB-LIFE	-	- -	-	1267/1268	-	0	3	8129	HRS	<37.317
FDI-1534		SN-4574	T.I.	LAB-LIFE	-	- -	-	/0371	-	1	70	500	HRS	28.571
FDI-1203	3F	SL1469	FAIRCHILD	LAB-CONT	-	-M-	-	0866/0967	-	1	5183	10921	HRS	0.018
FDI-1580	4G	N74/4A	SIGNETICS	LAB-CONT	-	M-M-	-	1169/0170	-	1	399	1644	HRS	1.524
FDI-1330	6E	8-8683	PHILCO	LAB-LIFE	-	M-M-	-	/0370	-	4	235	500	HRS	34.043
FDI-1534		U31994551A	FAIRCHILD	LAB-LIFE	-	M-M-	-	/0371	-	1	380	274	HRS	9.615
515.23 INTEGRATED-CIRCUITS,LOGIC-GATE														0.324 0.428 0.628
FDI-1313	6E	28884	PHILCO	LAB-LIFE	-	M-M-	-	/0769	-	0	7	671	HRS	<193.618
FDI-1534		245002-003	RADIATION	LAB-LIFE	-	M-M-	-	/0371	-	0	210	700	HRS	<5.515
FDI-1190	76	MC-930F	MOTOROLA	LAB-LIFE-CONT	-	M-M-	-	1267/0568	-	0	3	2516	HRS	<120.561
FDI-1214	76	PL-930-5U	PHILCO	LAB-LIFE	-	- -	-	1267/1268	-	0	3	8129	HRS	<37.317
FDI-1343	76	914301	FAIRCHILD	LAB-LIFE	-	M-M-	-	1267/1269	-	0	3	17184	HRS	<17.652
FDI-1343	76	SN15930	T.I.	LAB-LIFE	-	-M-	-	1267/1269	-	0	3	17184	HRS	<17.652
FDI-1214	76	SP839A	SIGNETICS	LAB-LIFE	-	M-M-	-	1267/1268	-	0	4	8129	HRS	<27.987
FDI-1343	76	PL9930-51	PHILCO	LAB-LIFE	-	-M-	-	1267/1269	-	0	3	17184	HRS	<17.652
FDI-1190	76	SG-211	SYLVANIA	LAB-LIFE-CONT	-	M-M-	-	1267/0568	-	0	3	2516	HRS	<120.561
FDI-1214	76	914301	FAIRCHILD	LAB-LIFE	-	M- -	-	1267/1268			3	8129		
FDI-1534		-10	ITT	LAB-LIFE	-	--	-	/0371			3/			
FDI-1214			PHILCO		-		-							

6.5 Operational/Non-Operational Failure Rate Comparison

A comparison of the failure rates for non-operational and operational environments was made using the non-operating model developed here and the MIL-HDBK-217B operational model. The comparison is presented in Figures 6-5 and 6-6. Failure rates for several operating conditions were predicted to present a range for comparison. The non-operating prediction was made at a nominal ambient temperature of 25 degrees centigrade.

Comparing the digital devices with aluminum metallization and aluminum wire gave an operating to non-operating ratio of 6 and 8 for Class A, small scale integration (SSI), digital devices at two operating junction temperatures: 35°C and 75°C; for Class B the ratios were 3 and 5; for Class C devices, 22 and 29; and for Class D, 82 and 108.

For medium scale integration (MSI), the ratios for Class A were 15 and 24; Class B, 8 and 14; Class C, 51 and 84; and Class D, 193 and 317.

Comparing the linear devices with aluminum metallization and aluminum wire gave an operating to non-operating ratio of 10 and 25 for Class A, small scale integration (SSI), linear devices at two operation junction temperatures: 35°C and 75°C; for Class B the ratios were 6 and 14; for Class C devices, 36 and 88; and for Class D, 133 and 329.

For medium scale integration (MSI), the ratios for Class A were 37 and 125; Class B, 21 and 71; Class C, 133 and 443; and Class D, 501 and 1662.

Failure rates for digital devices with aluminum metallization and gold wire were also compared. Since MIL-HDBK-217B uses one prediction model for both metallization systems, the operating failure rates are the same. For the non-operating failure rate, the aluminum metallization, gold wire systems exhibited a significantly higher failure rate, therefore the ratios are considerably different - so different that in some cases, the non-operating failure rate is higher than the

operating failure rate. The ratios for Class A, SSI Digital devices at the two junction temperatures are 0.6 and 0.8; for Class B, 0.4 and 0.5; for C, 2.2 and 2.9 and for Class D, 0.7 and 0.9.

For MSI devices, the ratios for Class A were 1.5 and 2.4; Class B, .8 and 1.4; Class C, 5.2 and 8.5; and Class D, 1.6 and 2.6.

Failure rates for linear devices with aluminum metallization and gold wire were also compared. For the non-operating failure rate, the aluminum metallization, gold wire systems exhibited a significantly higher failure rate, therefore the ratios are considerably different - so different that in some cases, the non-operating failure rate is higher than the operating failure rate. The ratios for Class A, SSI linear devices at the two junction temperatures are 1.0 and 2.5; for Class B, 0.6 and 1.4; for Class C, 3.6 and 8.8 and for Class D, 1.1 and 2.8.

For MSI devices, the ratios for Class A were 3.8 and 12.5; Class B, 2.2 and 7.1; Class C, 13.4 and 44.4; and Class D, 4.2 and 13.9.

Since most missile materiel are in the Class B or Class A quality range, average operating to non-operating factors can be defined as presented in Table 6-2.

DIGITAL OPERATING FAILURE RATES PER MIL-HDBK-217B*(GROUND FIXED ENVIRONMENT)

QUALTIY CLASS	CONDITION 1	CONDITION 2	CONDITION 3	CONDITION 4	PARTS COUNT
A	5.4	12.7	7.1	20.8	14.5
B	10.7	25.4	14.2	41.6	29.0
C	85.7	202.9	113.6	332.8	232.0
D	803.5	1901.9	1065.0	3120.0	2175.0

Condition 1
T_J = 35°C, 2 Gates
Condition 2
T_J = 35°C, 20 Gates
Condition 3
T_J = 75°C, 2 Gates
Condition 4
T_J = 75°C, 20 Gates

NON-OPERATING FAILURE RATE & NON-OPERATING/OPERATING RATIO

ALUMINUM METALLIZATION, ALUMINUM WIRE:

QUALITY CLASS	NON-OP FAILURE RATE*	RATIO CONDITION 1	RATIO CONDITION 2	RATIO CONDITION 3	RATIO CONDITION 4	PARTS COUNT
A	.875	6	15	8	24	17
B	3.06	3	8	5	14	9
C	3.94	22	51	29	84	59
D	9.84	82	193	108	317	221

ALUMINUM METALLIZATION, GOLD WIRE:

QUALITY CLASS	NON-OP FAILURE RATE*	RATIO CONDITION 1	RATIO CONDITION 2	RATIO CONDITION 3	RATIO CONDITION 4	PARTS COUNT
A	8.7	.6	1.5	.8	2.4	1.7
B	30.5	.4	.8	.5	1.4	1.0
C	39.3	2.2	5.2	2.9	8.5	5.9
D	1177.7	.7	1.6	.9	2.6	1.8

*Failures per Billion Hours.

FIGURE 6-5. MONOLITHIC BIPOLAR DIGITAL DEVICE OPERATIONAL/ NON-OPERATIONAL FAILURE RATE COMPARISON

LINEAR OPERATING FAILURE RATES PER MIL-HDBK-217B* (GROUND FIXED ENVIRONMENT)

QUALITY CLASS	CONDITION 1	CONDITION 2	CONDITION 3	CONDITION 4	PARTS COUNT
A	8.7	32.8	21.6	109.0	26.0
B	17.5	65.7	43.2	218.0	52.0
C	140.0	525.4	345.6	1744.0	416.0
D	1312.0	4926.0	3240.0	16350.0	3900.0

Condition 1
T_j = 35°C, 8 transistors
Condition 2
T_j = 35°C, 80 trabsistors
Condition 3
T_j = 75°C, 8 transistors
Condition 4
T_j = 75°C, 80 transistors

NON-OPERATING FAILURE RATE & NON-OPERATING/OPERATING RATIO

ALUMINUM METALLIZATION, ALUMINUM WIRE:

QUALITY CLASS	NON-OP FAILURE RATE*	RATIO CONDITION 1	RATIO CONDITION 2	RATIO CONDITION 3	RATIO CONDITION 4	PARTS COUNT
A	.875	10	37	25	125	30
B	3.06	6	21	14	71	17
C	3.94	36	133	88	443	106
D	9.84	133	501	329	1662	396

ALUMINUM METALLIZATION, GOLD WIRE:

QUALITY CLASS	NON-OP FAILURE RATE*	RATIO CONDITION 1	RATIO CONDITION 2	RATIO CONDITION 3	RATIO CONDITION 4	PARTS COUNT
A	8.7	1.0	3.8	2.5	12.5	3.0
B	30.5	.6	2.2	1.4	7.1	1.7
C	39.3	3.6	13.4	8.8	44.4	10.6
D	1177.7	1.1	4.2	2.8	13.9	3.3

*Failures per Billion Hours.

FIGURE 6-6. MONOLITHIC BIPOLAR LINEAR DEVICE OPERATIONAL/ NON-OPERATIONAL FAILURE RATE COMPARISON

TABLE 6-2.

AVERAGE OPERATING TO NON-OPERATING FAILURE RATE RATIO ALUMINUM METALLIZATION/ ALUMINUM WIRE

COMPLEXITY LEVEL	AVERAGE OPERATING TO NON-OPERATING FAILURE RATE RATIO	
	---Digital---	---Linear---
SSI	5	14
MSI	14	71

ALUMINUM METALLIZATION/GOLD WIRE

COMPLEXITY LEVEL	AVERAGE OPERATING TO NON-OPERATING FAILURE RATE RATIO	
	---Digital---	---Linear---
SSI	.5	1.4
MSI	1.4	7.1

The quality factors in the non-operating prediction model for a device with aluminum metal/gold wire systems were estimated from the aluminum metal/aluminum wire system.

SECTION 7

CONCLUSIONS AND RECOMMENDATIONS

The models developed can be used for predicting failure rates for monolithic bipolar SSI/MSI digital and linear integrated circuits.

The analysis indicates that a single metal should be used for the contact metallization and interconnection interface. The all-aluminum system shows a definitely more reliable storage capability than the aluminum metallization/gold wire system. Data on the Beam Lead Sealed Junction device with gold beams is not available on the linear devices.

In both user surveys and high temperature storage tests, wire bond failures were prominent.

For the aluminum metallization/aluminum wire systems, the principle problems were wire bonds and oxide defects or contamination.

Screens or tests recommended for wire bonds include centrifuge, temperature shock/cycling, power cycling, mechanical shock and bond pull tests. Due to the low mass of aluminum wires, the temperature shock/cycle, power cycle, and bond pull tests would be most effective.

Screens or tests recommended to weed out oxide defects include: Operating AC and DC with temperature; high temperature reverse bias; power cycling; elevated temperature storage; and visual inspection.

In the MIL-STD-883 screen, temperature cycling is required for Class A, B and C devices while temperature shock is only required for Class A devices. Burn-in and final electrical tests at maximum and minimum operating temperatures are required for Class A and B devices. Reverse bias burn-in is only required for Class A MOS and linear devices when specified. Visual inspection is required for Class A and B devices.

In quality conformance testing, bond pull tests, thermal shock, temperature cycling and high temperature storage are required for all quality classes.

Depending on whether Class A, B or C devices are specified in the procurement, it may be desirable to specify more screens and/or quality conformance tests which are related to wire bond and oxide reliability.

Field data has been collected for assemblies and missile systems indicating test equipment faults, mishandling, over voltage conditions during check out, etc. These result in assembly returns to depots or contractor repair facilities although no device failure or only secondary device failures are involved. This data will be analyzed in later reports; however, a preliminary evaluation indicates that the periodic checkout or cycling effects reliability primarily due to system test equipment and maintenance related problems rather than problems with the devices.

The evaluation assumes that the system design protects the devices from voltage surges or spikes inherent in the system and that the devices are derated to nominal values of 60 to 80% of output current and 60 to 75% of operating frequency.

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This report documents findings on the non-operating reliability of monolithic bipolar SSI/MSI digital & linear integrated circuits. Real time storage and accelerated testing results were analyzed and integrated to develop a non-operating reliability prediction model. Failure mechanisms are also discussed in detail. This information is part of a research program being conducted by the U. S. Army Missile R&D Command, Redstone Arsenal, AL. The objective of this program is the development of non-operating (storage) reliability

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prediction and assurance techniques for missile materiel. This report updates and replaces reports LC-76-IC1 and LC-76-IC2 dated May 1976.

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